PMICRO
Powerlink Microelectronics

PL51A003

Low Power High Performance ADC True EEPROM Flash 8051 MCU

Product Description:

PL51A003 is a microcontroller with ADC function integrated true EEPROM, built-in high-performance single cycle ET8051 core. This series of chips have 18 bidirectional universal I/O, support 16 interrupt sources (including 2 external interrupts), have 4 interrupt priorities.

For high reliability and low cost issues, PL51A003 builds in reliable watchdog timer (WDT), low power detect (LPD) and low voltage reset (LVR) function. The excellent noise immunity and ESD protection ensure reliable operations in the adverse electrical environments.

PL51T003 internal integrates low and high speed oscillators to operate and switch dynamically between a range of operating modes using different clock sources to optimize microcontroller operation and minimize power consumption.

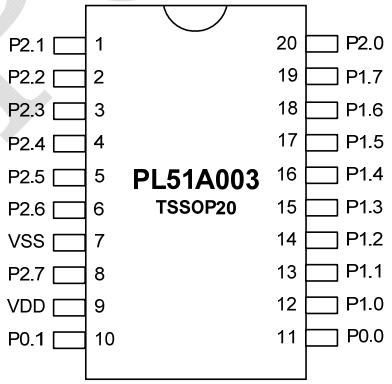
PL51A003 also supports three low power modes, idle mode, stop mode and sleep mode, to reduce power consumption. It supports to be wakeup speedy by Keyboard action when work in the low power mode.

PL51A003 Integrate UART0, UART1, SPI and I2C interfaces are built into the chip to provide users with interfaces to communicate with external hardware.

Besides the 16K bytes Flash program memory, other memory includes 256B RAM, 1KB XRAM and 256B data true EEPROM. Program and data area read control permissions can be configured, and the program area code encryption scrambling code storage, high security level to protect user program and data.

In-Circuit-Programming (ICP) supports the users to upgrade the program code and data in application board. ICD function supports debugging in application board.

For easy usage, POWERLINK provides the debugger and writer.



Key Features:

- 1T Enhanced 8-bit ET8051
- 16KB Flash
- 256B True EEPROM
- Operation Frequency@Voltage: ~12MHz@2.4~5.5V
- Operation Temperature: -25℃ ~+125℃
- Supports Crystal Oscillator, internal 32KHz and high precision RC oscillator(4/8/12MHz,± 2%@25℃), external clock input
- Programmable System Clock
- Up to 22 bidirectional GPIO
- Four Priority Levels with 16 interrupt sources
- 8 Keyboard Interrupts
- 2 External Interrupts
- Support POR/LVR/LPD
- Three 16-bit Timers/Counters
- Six 12-bit PWM: PWM0/1/2/3/4/5
- Three channels DBW
- Watchdog Timer with Prescaler
- Support UART0&1/SPI/I2C interface
- Integrated Analog Comparator
- Integrated 11bit 16 channels ADC
- Multi-mode Operation: Normal, Green, Stop, Sleep mode
- Support ICP&ICD
- Package: 24/20/16/8
- Memory Permission Control
- Flash Cycling: 100K@25℃
- EEPROM Cycling: 500K@25℃
- Data retention: 40 years@25℃

Applications:

- Wireless Mice, Keyboards and Game Controllers
- RF Remote Controller
- Small Home Appliances

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Product Types

Product Name	Package	Program Flash	Data EEPROM*5	RAM	Timer	PWM	Freq@Voltage	I/O	Interface UART/SPI/I2C	ACMP	T.S.	ADC
PL51A003B24	SSOP24	16KB	256B	256+1K	3	6+1	~12M@2.4~5.5V	22	2/1/1	1	1	16
PL51A003N24	QFN24											
PL51A003T20	TSSOP20	16KB	256B	256+1K	3	6+1		18	2/1/1	1	1	16
PL51A003N20	QFN20											
PL51A003S16	SOP16	16KB	256B	256+1K	3	6+1		14	1/1/1	1	1	9
PL51A003S8	SOP8	16KB	256B	256+1K	3	4		6	1/0/0	1	1	6

Note: *1: ACMP source, only between CMP1 and INTVREF (1.2V).

*2: Data area is true EEPROM.

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1 Overview

PL51A003 is a microcontroller with ADC function integrated true EEPROM, built-in high-performance single cycle ET8051 core. The PL51A003 series have a 22 bi-direction GPIO, a 16-source (including 2 external interrupt sources), 4-priority-level interrupt structure. .

For high reliability and low cost issues, PL51A003 builds in reliable watchdog timer (WDT), low power detect (LPD) and low voltage reset (LVR) functions. The excellent noise immunity and ESD protection ensure reliable operations in the adverse electrical environments.

PL51T003 integrates low and high frequency oscillators to operate and switch dynamically between a range of operating modes using different clock sources to optimize microcontroller operation and minimize power consumption.

In order to reduce power consumption, PL51A003 could be work in three low power modes, green IDLE mode, stop mode and sleep mode, it supports to be wakeup speedy by keyboard action when work in the low power mode.

PL51A003 is communicating with the outside world with UART0&1, I2C and SPI interfaces.

Besides the 16K bytes Flash program memory, other memory includes 256 bytes RAM Data Memory, 1K bytes XRAM Data Memory and 256 bytes true EEPROM Memory. Program and data area read control permissions can be configured, and the program area code encryption scrambling code storage, high security level to protect user program and data.

In-Circuit-Programming (ICP) support the users to upgrade the program code and data in circuit without removing the microcontroller from the actual application board.

In-Circuit-Debugging (ICD) support the users to debug the program code in circuit.

For easy usage, POWERLINK provides the debugger and writer.

PL51A003 is targeting at home appliance such as Wireless Mice, Keyboards and Game Controllers, RF Remote Controller, Induction cooker, Microwave oven, Washing machine, Clothes dryer, Dishwasher, Refrigerator, Air conditioner and etc.

2 Features

Basic

- 1T 8-bit ET8051 core
- Operating Voltage @ Frequency:
  - ~12MHz@2.4~5.5V
- Oscillator Type
  - Crystal Oscillator: 400KHz to 12MHz
  - Internal RC Oscillator: 4/8/12MHz (±2%@25℃) and 32KHz
  - External Clock: 400KHz to 12MHz
- Up to 22 bidirectional General Purpose I/O
  - Input-Only with configurable pull up/down resistor
  - Push-Pull Output Drive Capacity: 20mA (@5V, Total: <100mA)
- Operation Temperature: -25℃ to +125℃

Peripheral Features

- Four Priority Levels with 16 interrupt sources
  - Two External Interrupt: INT0B and INT1B(high/low level, edge wakeup)
  - T0&T1 Overflow Interrupt
  - T2 Overflow, Reload, Compare/Capture Interrupt
  - UART0&1 Transmit and Receive Interrupt
  - EEPROM Write Finished Interrupt
  - Analog Comparator Interrupt
  - Keyboard Interrupt
  - SPI Interrupt
  - I2C Interrupt
  - ADC Finish Converting Interrupt
  - LPD Interrupt
- POR/LVR/LPD support
- Eight LVR threshold Level by Fuse:
  - 1.2/1.5/1.8/2.1/2.4/3.7/4.3 V
- Eight LPD threshold Level by Fuse:
  - 1.2/1.5/1.8/2.1/2.4/3.7/4.3 V
- Register Timed Access Protection
- Programmable System Clock
- Multi-mode Operation:
  - Normal/Idle/Stop/Sleep
- 16-bit Timers/Counters:
  - 80C51-like Timer 0 & 1
  - 8052-like Timer 2 with Compare/Capture Unit (CCU)
- Six 12-bit PWM: PWM0/1/2/3/4/5
  - PWM0/3 share period and control register
  - PWM1/4 share period and control register
  - PWM2/5 share period and control register
  - Four output mode: standard, center-aligned, register matched set high level and toggled.
- Three channels DBW
  - Rising edge, falling edge deadband control

- ✓ Multiple signal source select
- ✧ BEEPER: 1/2/4 KHz
- ✧ Watchdog Timer with Additional Configurable Prescaler: WDT
- ✧ UART0/UART1/SPI/I2C Interface
- ✧ Analog Digital Converter: ADC
  - ✓ 11-bit resolution
  - ✓ Up to 16 multiplexed channels
  - ✓ Support scan mode and continuous conversion mode
  - ✓ Support external input VREF
- ✧ Analog Comparator: ACMP
- ✧ Support In-Circuit Programming: ICP
- ✧ Support In-Circuit Debugging: ICD
- ✧ ESD: >4KV (HBM)
- ✧ EFT: >4KV
- ✧ Package Types
  - ✓ SSOP24/QFN24
  - ✓ TSSOP20/QFN20
  - ✓ SOP16/SOP8

Memory

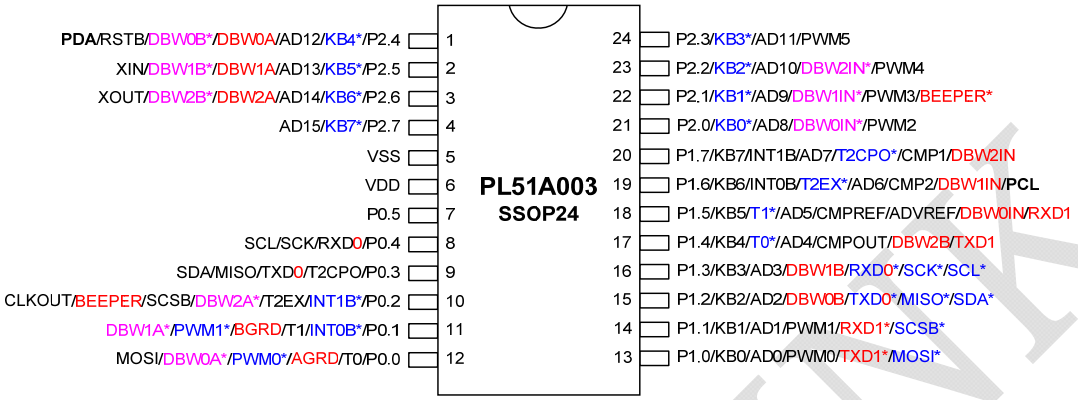
- ✧ 16K bytes Program Flash
- ✧ 256 bytes Data EEPROM（byte/page operation, 1page=64bytes)
- ✧ 256 bytes internal scratch-pad RAM
- ✧ 1K bytes internal XRAM
- ✧ Memory Programming Permission Control
- ✧ Flash Cycling: 100K@25℃
- ✧ EEPROM Cycling: 500K@25℃
- ✧ Data retention: 40 years@25℃

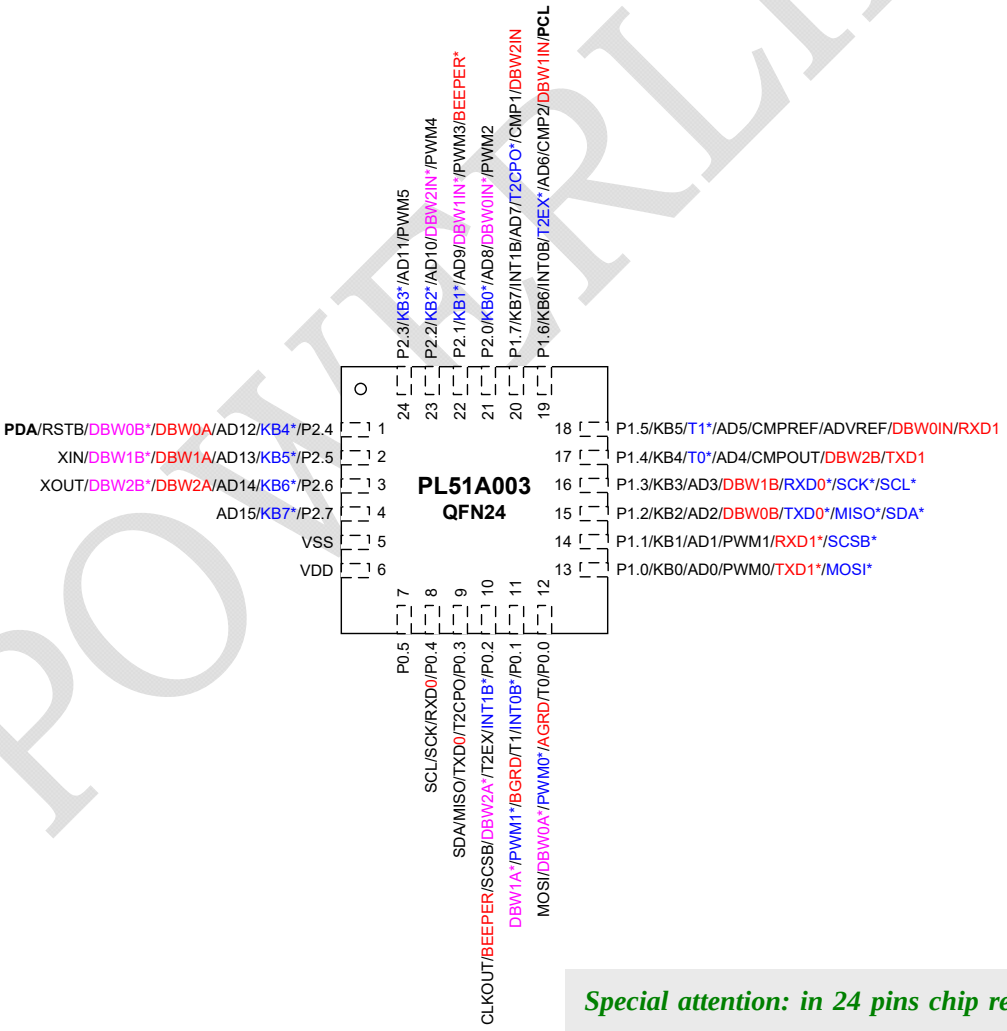
3 Quick Reference Data

Parameter	Value	Units
Min Supply Voltage	2.4	V
Operating Temperature Range	-25 to +125	℃
Internal RC OSC Frequency	4/8/12	MHz
Internal RC OSC Precision @ 25℃	±2	%
Push-Pull Output Drive Capacity @ 5V	20	mA
Push-Pull Output Drive Capacity @ 3.3V	10	mA
Total Push-Pull Output Drive Capacity	<100	mA
Current Consumption @ Sleep Mode	3	uA

4 Pin Configurations

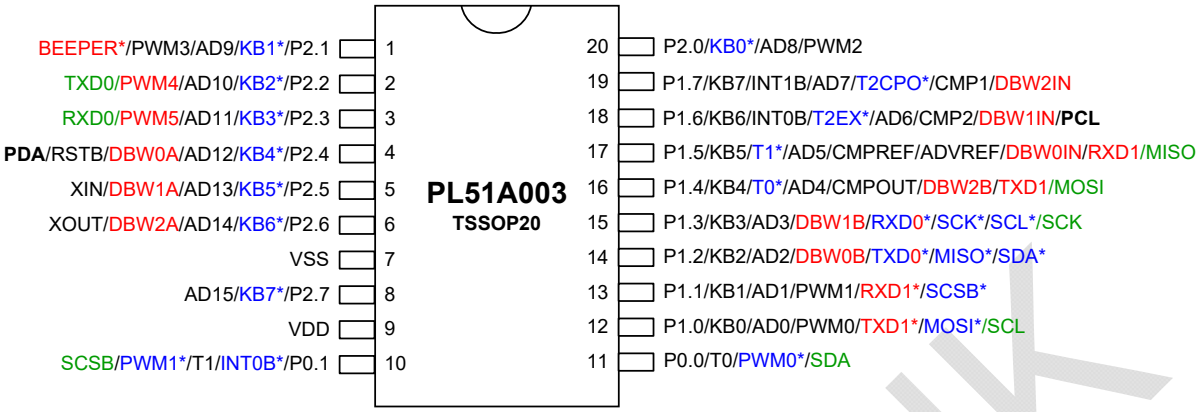
4.1 Pin Diagrams (24 Pin)

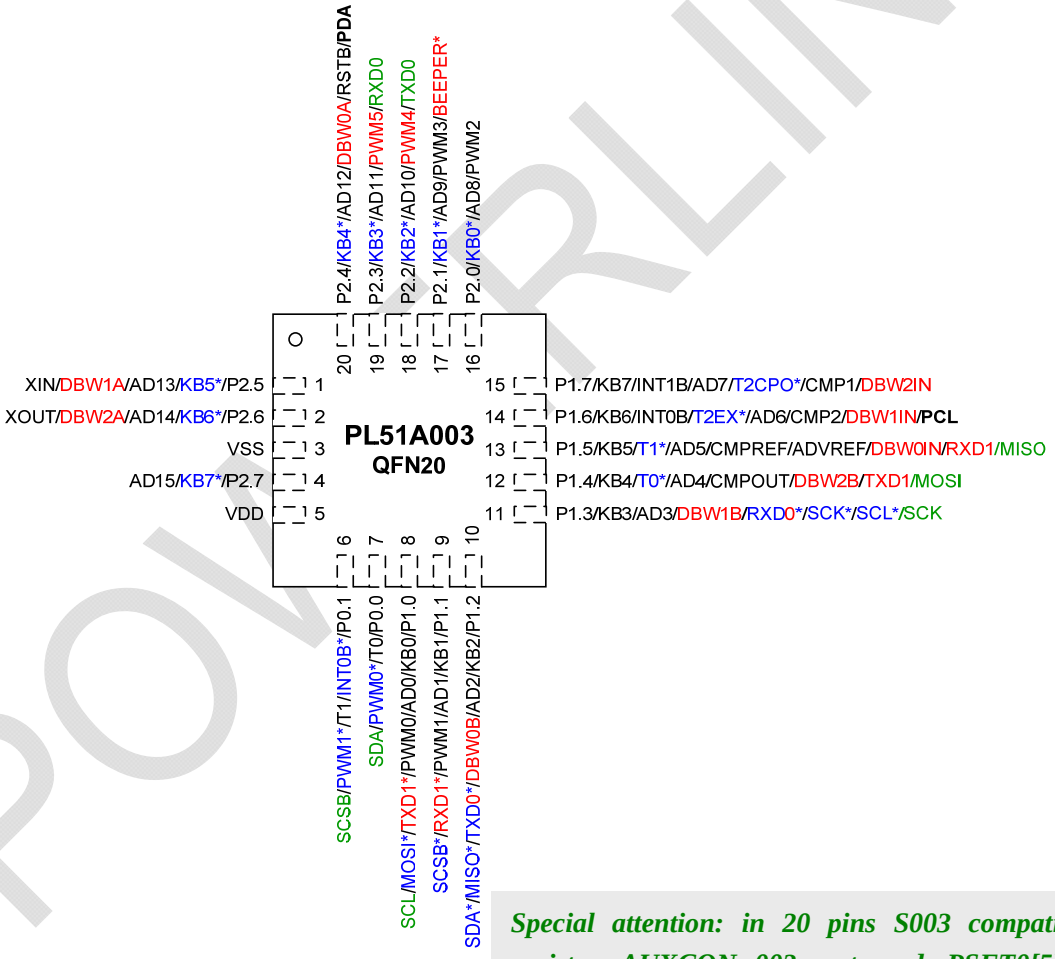




Special attention: in 24 pins chip register AUXCON.s003_sopt cannot be set to 1.

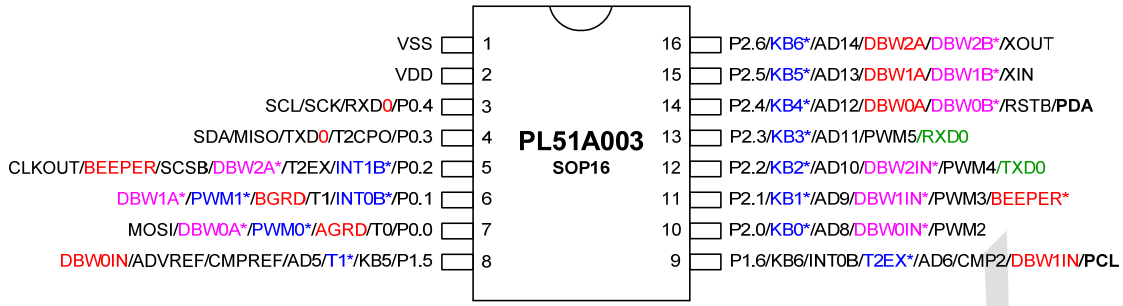
4.2 Pin Diagrams (20 Pin)





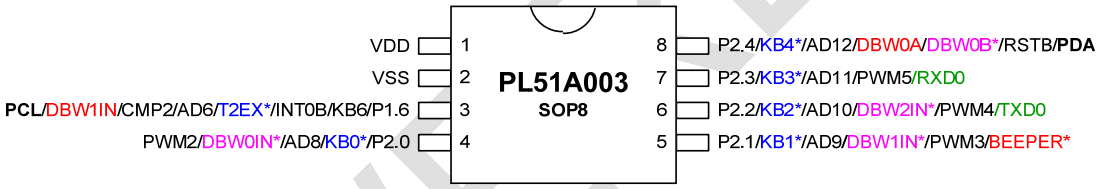
Special attention: in 20 pins S003 compatible chip, register AUXCON.s003_sopt and PSFT0[5](UART0) cannot be set to 1 at the same time.

4.3 Pin Diagrams (16 Pin)



Special attention: in 16 pins chip, when register AUXCON.s003_sopt is 1, PSFT0[5] must be set to 1.
In addition, when s003_sopt is 1 UART0 shift to green pin, SPI/I2C synchronously shift to undesired pin result in SPI/I2C invalid, generally not recommend.

4.4 Pin Diagrams (8 Pin)



Note:

1) The outside pin function has the highest priority, and the inner pin function has the lowest priority. It means that if the higher priority function is enabled, the lower priority function can't be used even when the lower priority function is also enabled.

2) The pin name colored blue with * denoted the shift ports, the pin function available only when the relative shift control bit in SFR "PSFT0~1" is set.

3) The green pins are S003 compatible pin definition: if register AUXCON.s003_sopt set as 1, the SPI/I2C/UART0 will shift to the corresponding green pin at same time, the original SPI/I2C/UART0 and its shift pin function are disabled. (*pay attention to the special attention of different type of package pin*)

4) For unused or not led out pins, recommended to configure input pull-up or output fixed lever.

4.5 Pin Description

Symbol	Type	Descriptions
VDD	Power	Power Supply (2.0~5.5V)
VSS	Power	Ground (0V)
RSTB	Digital Input	Reset Pin, Active Low
XIN	Analog Input	Crystal Oscillator Input
XOUT	Analog Output	Crystal Oscillator Output
CLKOUT	Digital Output	Internal Clock Output
SCL	Digital I/O	Clock for I2C Interface
SDA	Digital I/O	Data I/O for I2C Interface
SCSB	Digital Input	Enable Input for SPI Interface, active Low
SCK	Digital I/O	Clock for SPI Interface
MISO	Digital I/O	Master Data Input or Slave Data Output for SPI Interface
MOSI	Digital I/O	Master Data Output or Slave Data Input for SPI Interface
RXD0/1	Digital Input	RXD0/1 of Serial Port
TXD0/1	Digital Output	TXD0/1 of Serial Port
T0	Digital Input	Timer 0 Input
T1	Digital Input	Timer 1 Input
T2EX	Digital Input	Timer 2 External Capture Input
T2CPO	Digital Output	Timer 2 Compare/PWM Ouput
INT0B	Digital Input	External Interrupt 0
INT1B	Digital Input	External Interrupt 1
PWM0	Digital Output	PWM 0 Output
PWM1	Digital Output	PWM 1 Output
PWM2	Digital Output	PWM 2 Output
PWM3	Digital Output	PWM 3 Output
PWM4	Digital Output	PWM 4 Output
PWM5	Digital Output	PWM 5 Output
DBW0A	Digital Output	Deadband Waveform Generation DBW0A Output
DBW1A	Digital Output	Deadband Waveform Generation DBW1A Output
DBW2A	Digital Output	Deadband Waveform Generation DBW2A Output
DBW0B	Digital Output	Deadband Waveform Generation DBW0B Output
DBW1B	Digital Output	Deadband Waveform Generation DBW1B Output
DBW2B	Digital Output	Deadband Waveform Generation DBW2B Output
DBW0IN	Digital Input	Deadband Waveform Generation DBW0 Input
DBW1IN	Digital Input	Deadband Waveform Generation DBW1 Input
DBW2IN	Digital Input	Deadband Waveform Generation DBW2 Input
CMP1	Analog Input	Comparator Positive 1 Input
CMP2	Analog Input	Comparator Positive 2 Input

Symbol	Type	Descriptions
CMPVREF	Analog Input	Comparator Reference Voltage Input
CMPOUT	Digital Output	Comparator Output
KB0~7	Analog Input	Keyboard Inputs
ADVREF	Analog Input	ADC Reference Voltage Input
AD0~AD15	Analog Input	16 Channels ADC Inputs
BEEPER	Digital Output	BEEPER Output
P0.0~P0.5	Digital I/O	General purpose I/O Port 0
P1.0~P1.7	Digital I/O	General purpose I/O Port 1
P2.0~P2.7	Digital I/O	General purpose I/O Port 2
PCL	Digital Input	Clock Input for ICP (In Circuit Program) Mode
PDA	Digital I/O	Data I/O for ICP (In Circuit Program) Mode

4.6 Terminology and Symbol Conventions

Symbol	Description	Symbol	Description
CPU	Control Processor Unit	**PFL**	Program Flash
ALU	Arithmetic-Logic Unit	**DEE**	Data EEPROM
MSB	Most Significant Bit	**NVR**	NVR EEPROM
LSB	Least Significant Bit	**CEE**	Code Fuse EEPROM
SFR	Special Function Register	**TEE**	Trim Fuse EEPROM
ISR	Interrupt Service Routine unit	**ICP**	In-Circuit Programming
POR	Power On Reset	**ICD**	In-Circuit Debugging
LVR	Low Voltage Reset	**ISP**	In-System Programming
LPD	Low Power Detect	**TW**	Write operation is permitted only after open a window by 'TA' register
PMU	Power Management Unit	**SPI**	Serial Peripheral Interface
PWM	Pulse Width Modulation	**I2C**	Two-Wire Interface
WDT	Watch Dog Timer	**UART**	Universal Asynchronous Receiver Transmitter
CCU	Compare/Capture Unit	**ADC**	Analog Digital Converter
TA	Timed Access	**ACMP**	Analog Comparator
DBW	Deadband Waveform Generator	**CAP**	Capacitive Touch Sensor

Symbol	Description	Symbol	Description
TSC	Temperature Detect Sensor	**TKC**	Touch Capacitive Sensor

5 Block Diagram

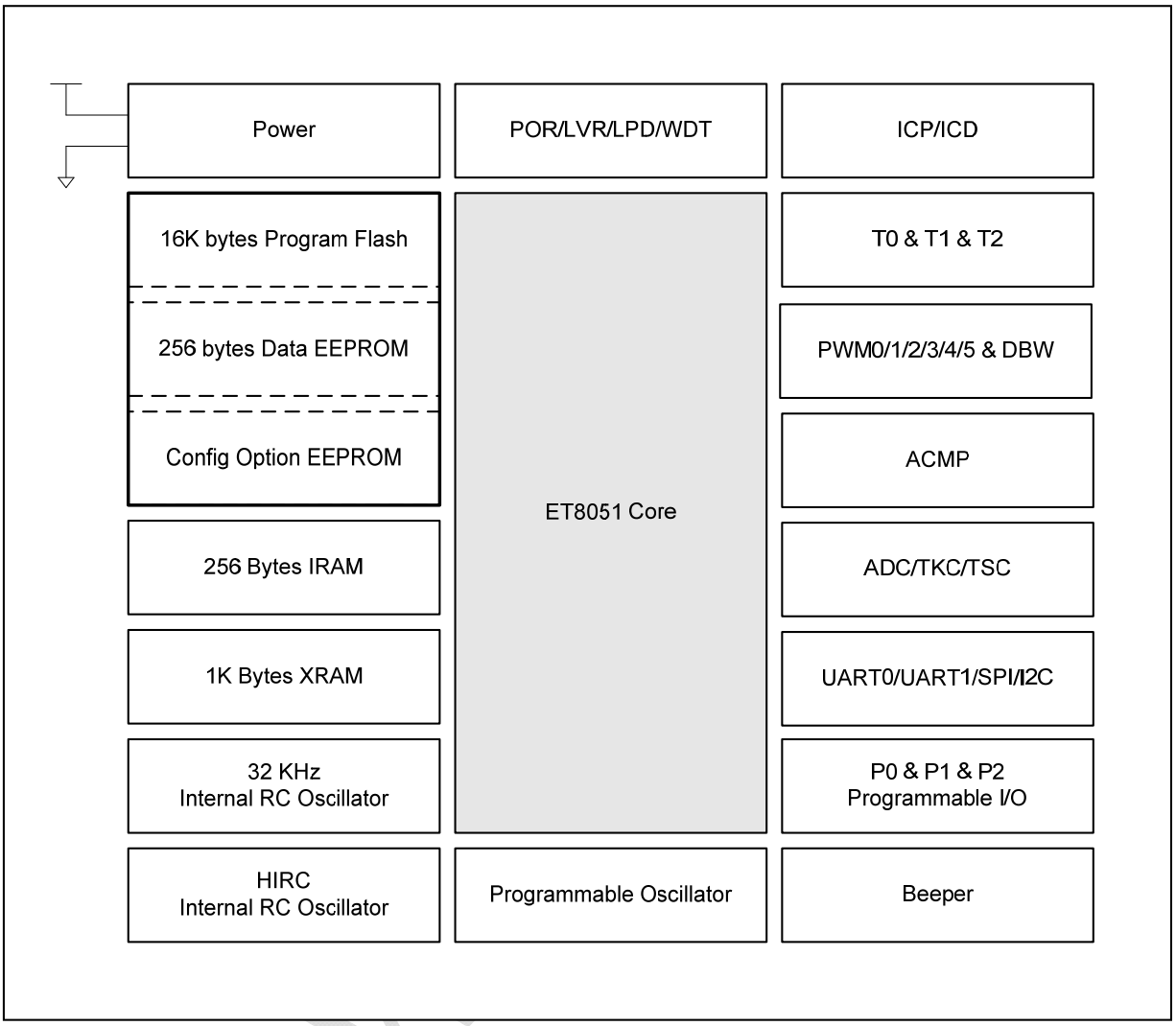


Figure 5-1 Block diagram

6 Memory Organization

The ET8051 microcontroller core incorporates the Harvard architecture, with separate code and data spaces.

Memory organization in the ET8051 is similar to that of the industry standard 8051. There are three memory areas: Program Memory (Internal FLASH), External Data Memory (External EEPROM) and Internal Data Memory (Internal RAM).

The Program Memory includes 16K bytes program FLASH.

The External Data Memory includes 1K bytes XRAM and 256 bytes data EEPROM.

The Internal Data Memory includes 256 bytes internal scratch-pad RAM.

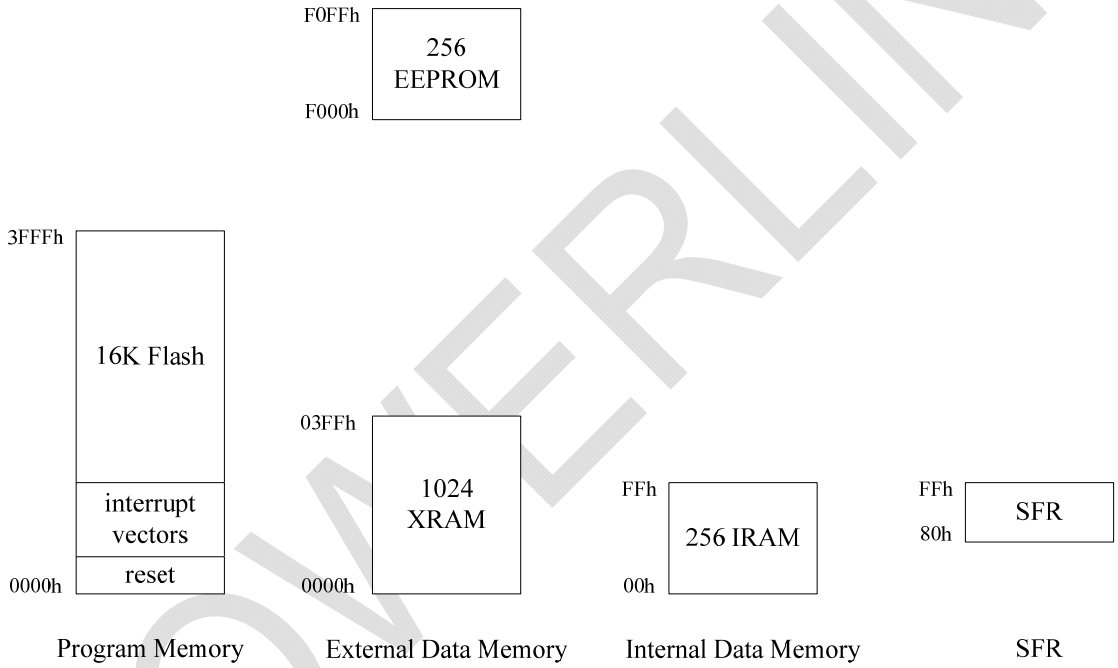


Figure 6-1 Memory Map

6.1 Program Memory

Program memory is used for storing program code, after reset, the CPU starts program execution at location 0000h. The lower part of program memory includes interrupt and reset vectors. The interrupt vectors are spaced at 8-byte intervals, starting from 0003h.

6.2 External Data Memory

External data memory is used for data storage.

The 256 bytes data memory, it's address mapped into F000h~F0FFh.

The external data memory also contains 1024 bytes of XRAM, via PCON.PGSEL<1:0> as the page selection bit of XRAM. When using 8-bit MOVX addressing, the page selection bit provides the high level of the 16 bit address, the high 6-bits of the address are always 0, and the memory is 256 bytes for one page.

6.3 Data Pointer Registers

Data pointers accelerate data blocks moving. Data Pointer Register (DPTR) is a 16-bit register that is used to address external memory or peripherals.

The ET8051 includes one Data Pointer Register. The active Data Pointer Register can be accessed as SFRs: DPH, DPL.

6.4 Internal Data Memory

The internal data memory interface services up to 256 bytes data memory. The memory space accommodates also 128 bytes of Special Function Registers.

Indirect addressing access memory address space upper 128 bytes (7Fh~FFh), and direct addressing can access SFR address space higher than 7Fh.

The lower 128 bytes contain work registers (00h … 1Fh) and bit-addressable memory (20h … 2Fh). The lowest 32 bytes form four banks, each consisting of eight registers (R0-R7). Two bits of the program memory status word (PSW) select which bank is in use. The next 16 bytes of memory form a block of bit-addressable memory, accessible via 00h-7Fh addresses.

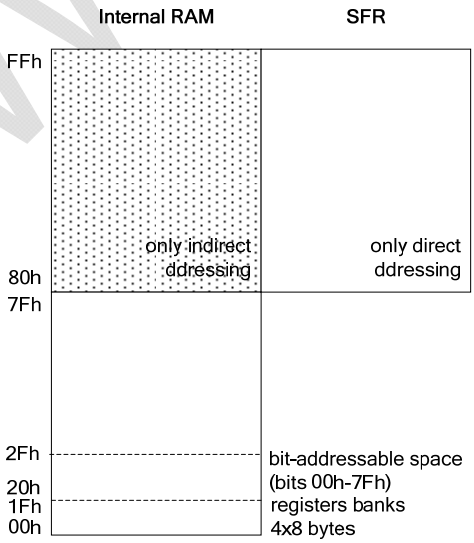


Figure 6-2 Internal Memory Map

7 Special Function Registers

7.1 Special Function Registers Locations

The map of Special Function Registers is shown in the following Table. Some addresses are occupied, while the others are not implemented. Read & write access to unimplemented addresses will target the External SFR Interface.

Table 7-1 Special Function Registers Locations

Hex/ Bin	X000	X001	X010	X011	X100	X101	X110	X111	Bin/ Hex
F8	RSTCON	PWMEN	PWM0CON	PWM0PL	PWM0PH	PWM0DL	PWM0DH	TA	**FF**
F0	B		PWM1CON	PWM1PL	PWM1PH	PWM1DL	PWM1DH	SRST	**F7**
E8	AUXCON		PWM2CON	PWM2PL	PWM2PH	PWM2DL	PWM2DH		**EF**
E0	ACC	PWM5DL	PWM5DH	PWM4DL	PWM4DH	PWM3DL	PWM3DH		**E7**
D8	ADGRD	ADWKL0	ADWKH0	ADWKL1	ADWKH1	ADSTA		ADTCSOF	**DF**
D0	PSW	ADDATL	ADDATH	ADCHS0	ADCHS1	ADCON0	ADCON1	ADCON2	**D7**
C8	T2CON	T2MOD	CRCL	CRCH	TL2	TH2	ADOUTL	ADOUTH	**CF**
C0	IRCON	DBWDB0	DBWDB1	DBWCON0	DBW0CON1	DBW0CON2	DBW1CON1	DBW1CON2	**C7**
B8	IE1	IP1L	IP1H	DBW2CON0	DBW2CON1	DBW2CON2	CMPCON1	CMPCON0	**BF**
B0	SPICON	SPIDAT	SPISTA		I2CADR	I2CDAT	I2CSTA	I2CCON	**B7**
A8	IE0	IP0L	IP0H	PRASW	P1ASW	P2ASW	PSFT0	PSFT1	**AF**
A0	P2	P0M0	P0M1	P1M0	P1M1	P2M0	P2M1	KBCON	**A7**
98	S0CON	S0BUF	S0BDL	S0BDH	S1BUF	S1BDL	S1BDH	S1CON	**9F**
90	P1	BEEPER			PLLCON	SCSCON	SCKCON	EECON	**97**
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	TCKCON	**8F**
80	P0	SP	DPL	DPH	TREGC	TREGD	WDTCON	PCON	**87**

The 16 addresses from SFR space are both byte- and bit-addressable. The bit-addressable SFRs are registers which addresses end with 000’b (80’h, 88’h, 90’h … F8’h). Those 16 registers (128 bits) together with 128 bits from internal data memory (locations 20’h … 2F’h) form the bit-addressable space.

Table 7-2 Bit-addressable Space

Hex/ Bin	X000	X001	X010	X011	X100	X101	X110	X111	Bin/ Hex
SFR									
F8									**FF**
F0									**F7**
E8									**EF**
E0									**E7**
D8									**DF**
D0									**D7**
C8									**CF**
C0									**C7**
B8									**BF**
B0									**B7**
A8									**AF**
A0									**A7**
98									**9F**
90									**97**
88									**8F**
80									**87**
Hex/ Bin	**X000**	**X001**	**X010**	**X011**	**X100**	**X101**	**X110**	**X111**	**Bin/ Hex**
Internal RAM									
78	2Fh.0	2Fh.1	2Fh.2	2Fh.3	2Fh.4	2Fh.5	2Fh.6	2Fh.7	**7F**
70	2Eh.0	2Eh.1	2Eh.2	2Eh.3	2Eh.4	2Eh.5	2Eh.6	2Eh.7	**77**
68	2Dh.0							2Dh.7	**6F**
60	2Ch.0							2Ch.7	**67**
58	2Bh.0							2Bh.7	**5F**
50	2Ah.0							2Ah.7	**57**
48	29h.0							29h.7	**4F**
40	28h.0							28h.7	**47**
38	27h.0							27h.7	**3F**
30	26h.0							26h.7	**37**
28	25h.0							25h.7	**2F**
20	24h.0							24h.7	**27**
18	23h.0							23h.7	**1F**
10	22h.0							22h.7	**17**
08	21h.0	21h.1	21h.2	21h.3	21h.4	21h.5	21h.6	21h.7	**0F**
00	20h.0	20h.1	20h.2	20h.3	20h.4	20h.5	20h.6	20h.7	**07**

7.2 Special Function Registers Reset Values

Table 7-3 Special Function Registers Reset Values

SFR	ADR	B7	B6	B5	B4	B3	B2	B1	B0	RST
CPU										
ACC	E0H	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	00H
B	F0H	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	00H
PSW	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00H
SP	81H	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0	07H
DPH	83H	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0	00H
DPL	82H	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0	00H
CKCON	8EH	CKCON.7	CKCON.6	CKCON.5	CKCON.4	CKCON.3	CKCON.2	CKCON.1	CKCON.0	88H
TA	FFH	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0	FFH
Clock Control										
SCKCON	96H	D7	D6	D5	D4	D3	D2	D1	D0	00h
SCSCON	95H	SOSCSW	OSC2EN	SOSC.5	SOSC.4	SOSC.3	SOSC.2	SOSC.1	SOSC.0	00h
PLLCON	94H	PLLEN	PLLFR	-	PLLCON.4	PLLCON.3	PLLCON.2	PLLCON.1	PLLCON.0	40h
Reset Control										
RSTCON	F8H	-	-	FCHK	LPDF	PORF	LVRF	EXRF	WDRF	28h
SRST	F7H	-	-	-	-	-	-	-	D0	00h
Power Control										
PCON	87H	PGSEL1	PGSEL0	ISR_TM	PMW	P2SEL	SLEEP	STOP	IDLE	08h
Interrupt Control										
IE0	A8H	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	00h
IE1	B8H	ET2R	ELPD	ETK	EKB	ET2C	ECMP	ESPI	EI2C	00h
IRCON	C0H	T2RF	TF2	TKF	KBF	T2CF	CMPF	-	-	00h
IP0	A9H	PEEL	PS1L	PT2L	PS0L	PT1L	PX1L	PT0L	PX0L	00h
IP0H	AAH	PEEH	PS1H	PT2H	PS0H	PT1H	PX1H	PT0H	PX0H	00h
IP1	B9H	PT2RL*	PLPDL	PTKL	PKBL	PT2CL	PCMPL	PSPIL	PI2CL	00h
IP1H	BAH	PT2RH*	PLPDH	PTKH	PKBH	PT2CH	PCMPH	PSPIH	PI2CH	00h
Keyboard Control										
KBCON	A7H	D7	D6	D5	D4	D3	D2	D1	D0	00h
Port Control										
P0	80H	-	-	D5	D4	D3	D2	D1	D0	00h
P0M0	A1H	-	-	D5	D4	D3	D2	D1	D0	00h

SFR	ADR	B7	B6	B5	B4	B3	B2	B1	B0	RST
P0M1	A2H	-	-	D5	D4	D3	D2	D1	D0	00h
P1	90H	D7	D6	D5	D4	D3	D2	D1	D0	00h
P1M0	A3H	D7	D6	D5	D4	D3	D2	D1	D0	00h
P1M1	A4H	D7	D6	D5	D4	D3	D2	D1	D0	00h
P2	A0H	D7	D6	D5	D4	D3	D2	D1	D0	00h
P2M0	A5H	D7	D6	D5	D4	D3	D2	D1	D0	00h
P2M1	A6H	D7	D6	D5	D4	D3	D2	D1	D0	00h
P1ASW	ACH	D7	D6	D5	D4	D3	D2	D1	D0	00h
P2ASW	ADH	D7	D6	D5-	D4	D3	D2	D1	D0	00h
PSFT0	AEH	SPI	I2C	UART0	INT1B	INT0B	T2	T1	T0	00h
PSFT1	AFH	-	DBW	UART1	BEEPER	KEYB	TKCH	PWM1	PWM0	00H
PRASW	ABH	-	P2RSW	P1RSW	P0RSW	P0ASW.3	P0ASW.2	P0ASW.1	P0ASW.0	00H
Timer0/1/2Control										
TCON	88H	TF1	TR1	TF0	TR0	IF1	IT1	IF0	IT0	00h
TMOD	89H	T1Gate	T1c/t	T1M1	T1M0	T0Gate	T0c/t	T0M1	T0M0	00h
TCKCON	8FH	-	T2PS2	T2PS1	T2PS0	T1PS1	T1PS0	T0PS1	T0PS0	4Fh
TH0	8CH	D7	D6	D5	D4	D3	D2	D1	D0	00h
TL0	8AH	D7	D6	D5	D4	D3	D2	D1	D0	00h
TH1	8DH	D7	D6	D5	D4	D3	D2	D1	D0	00h
TL1	8BH	D7	D6	D5	D4	D3	D2	D1	D0	00h
T2CON	C8H	T2EN	AES1	AES0	T2R1	T2R0	T2CM	IT1_INV	INT0_INV	00h
T2MOD	C9H	S0BDS	S0BDD	LSMSR	-	-	D2	D1	D0	00h
CRCH	CBH	D7	D6	D5	D4	D3	D2	D1	D0	00h
CRCL	CAH	D7	D6	D5	D4	D3	D2	D1	D0	00h
TH2	CDH	D7	D6	D5	D4	D3	D2	D1	D0	00h
TL2	CCH	D7	D6	D5	D4	D3	D2	D1	D0	00h
PWM Control										
PWMEN	F9H	-	-	PWM5EN	PWM4EN	PWM3EN	PWM2EN	PWM1EN	PWM0EN	00h
PWM0CON	FAH	PWM0DS	PWM0MS1	PWM0MS0	PWM0CS1	PWM0CS0	PWM0PS2	PWM0PS1	PWM0PS0	00h
PWM1CON	F2H	PWM1DS	PWM1MS1	PWM1MS0	PWM1CS1	PWM1CS1	PWM1PS2	PWM1PS1	PWM1PS0	00h
PWM2CON	EAH	PWM2DS	PWM2MS1	PWM2MS0	PWM2CS1	PWM2CS1	PWM2PS2	PWM2PS1	PWM2PS0	00h
PWM0PH	FCH	-	-	-	-	D3	D2	D1	D0	00h
PWM0PL	FBH	D7	D6	D5	D4	D3	D2	D1	D0	00h
PWM0DH	FEH	-	-	-	-	D3	D2	D1	D0	00h
PWM0DL	FDH	D7	D6	D5	D4	D3	D2	D1	D0	00h

SFR	ADR	B7	B6	B5	B4	B3	B2	B1	B0	RST
PWM1PH	F4H	-	-	-	-	D3	D2	D1	D0	00h
PWM1PL	F3H	D7	D6	D5	D4	D3	D2	D1	D0	00h
PWM1DH	F6H	-	-	-	-	D3	D2	D1	D0	00h
PWM1DL	F5H	D7	D6	D5	D4	D3	D2	D1	D0	00h
PWM2PH	ECH	-	-	-	-	D3	D2	D1	D0	00h
PWM2PL	EBH	D7	D6	D5	D4	D3	D2	D1	D0	00h
PWM2DH	EEH	-	-	-	-	D3	D2	D1	D0	00h
PWM2DL	EDH	D7	D6	D5	D4	D3	D2	D1	D0	00h
PWM3DH	E6H	-	-	-	-	D3	D2	D1	D0	00h
PWM3DL	E5H	D7	D6	D5	D4	D3	D2	D1	D0	00h
PWM4DH	E4H	-	-	-	-	D3	D2	D1	D0	00h
PWM4DL	E3H	D7	D6	D5	D4	D3	D2	D1	D0	00h
PWM5DH	E2H	-	-	-	-	D3	D2	D1	D0	00h
PWM5DL	E1H	D7	D6	D5	D4	D3	D2	D1	D0	00h
WDT Control										
WDTCON	86H	WDTEN	-	WDTIEN	WDTIF	WDTPS3	WDTPS2	WDTPS1	WDTPS0	00h/80h
UART0 Control										
S0CON	98H	S0M0	S0M1	S0M2	REN0	TB80	RB80	TI0	RI0	00h
S0BUF	99H	D7	D6	D5	D4	D3	D2	D1	D0	00h
S0BDL	9AH	D7	D6	D5	D4	D3	D2	D1	D0	D9h
S0BDH	9BH	-	-	-	-	-	-	D1	D0	03h
UART1 Control										
S1CON	9FH	S1M0	-	S1M2	REN1	TB81	RB81	TI1	RI1	00h
S1BUF	9CH	D7	D6	D5	D4	D3	D2	D1	D0	00h
S1BDL	9DH	D7	D6	D5	D4	D3	D2	D1	D0	00h
S1BDH	9EH	-	-	-	-	-	-	D1	D0	03h
SPI Control										
SPSTA	B2H	SPIF	WCOL	SSERR	MODF	-	-	-	-	00h
SPCON	B0H	SPR2	SPEN	SSDIS	MSTR	CPOL	CPHA	SPR1	SPR0	14h
SPDAT	B1H	D7	D6	D5	D4	D3	D2	D1	D0	00h
I2C Control										
I2CSTA	B6H	D7	D6	D5	D4	D3	D2	D1	D0	F8h
I2CCON	B7H	CR2	ENS1	STA	STO	SI	AA	CR1	CR0	00h
I2CDAT	B5H	D7	D6	D5	D4	D3	D2	D1	D0	00h
I2CADR	B4H	ADR.6	ADR.5	ADR.4	ADR.3	ADR.2	ADR.1	ADR.0	GC	00h

SFR	ADR	B7	B6	B5	B4	B3	B2	B1	B0	RST
ADC Control										
ADWKL0	D9H	D7	D6	D5	D4	D3	D2	D1	D0	00h
ADWKH0	DAH	D7	D6	D5	D4	D3	D2	D1	D0	00h
ADWKL1	DBH	D7	D6	D5	D4	D3	D2	D1	D0	00h
ADWKH1	DCH	D7	D6	D5	D4	D3	D2	D1	D0	00h
ADDATL	D1H	D7	D6	D5	D4	D3	D2	D1	D0	00h
ADDATH	D2H	D7	D6	D5	D4	D3	D2	D1	D0	00h
ADCHS0	D3H	D7	D6	D5	D4	D3	D2	D1	D0	00h
ADCHS1	D4H	D7	D6	D5	D4	D3	D2	D1	D0	00h
ADCON0	D5H	TKC_EN	ADC_EN	TSC_EN	WAIT_ TKRD_EN	FREQ_ SEL2	FREQ_ SEL1	FREQ_ SEL0	SCAN_ MODE	00h
ADCON1	D6H	START	ACCUM_ SEL2	ACCUM_ SEL1	ACCUM_ SEL0	AVG_DIS	TRIG_SEL	FUNC_ FLAG	ACCUM_ OVF	00h
ADCON2	D7H	LSLP_ MODE	SES_GAP 2	SES_GAP 1	SES_GAP 0	IDLE_ RUN_FLA G	WAIT_ TKRD_FL AG	STA_GAP 1	STA_GAP 0	00h
ADSTA	DDH	INJECT	ADC_PU MP	IREF_ADJ 1	IREF_ADJ 0	ADC_CC M	ADC_VRE F2	ADC_VRE F1	ADC_VRE F0	00h
ADCSOF	DFH	-	CPOL	CH_SW1	CH_SW0	ESCAP_ OFST3	ESCAP_ OFST2	ESCAP_ OFST1	ESCAP_ OFST0	0Fh
ADOUTL	CEH	D7	D6	D5	D4	D3	D2	D1	D0	00h
ADOUTH	CFH	-	-	-	-	-	D2	D1	D0	00h
Analog Comparator Control										
CMPCON0	BFH	CEN	CPS	CNS	OEN	CPO	DBT	SYN	HSY	00h
CMPCON1	BEH	TGS3	TGS2	TGS1	TGS0	VREF_EN	CDS2	CDS1	CDS0	00h
EEPROM Control										
EECON	97H	LOCK	FUSE	DENC	DSCR	EPGM	PGMF	CPF	PGM	00h
Test Register										
TREGC	84H	-	-	D5	D4	D3	D2	D1	D0	00h
TREGD	85H	D7	D6	D5	D4	D3	D2	D1	D0	00h
DBW Register										
DBWDB0	C1H	-	-	DBWDB0. 5	DBWDB0. 4	DBWDB0. 3	DBWDB0. 2	DBWDB0. 1	DBWDB0. 0	00h
DBWDB1	C2H	-	-	DBWDB1. 5	DBWDB1. 4	DBWDB1. 3	DBWDB1. 2	DBWDB1. 1	DBWDB1. 0	00h

SFR	ADR	B7	B6	B5	B4	B3	B2	B1	B0	RST
DBWCON0	C3H	G1EN	G1POLB	G1POLA	G1CS0	G0EN	G0POLB	G0POLA	G0CS0	00h
DBW0CON1	C4H	G0ASDLB1	G0ASDLB0	G0ASDLA1	G0ASDLA0	G0IS.3	G0IS.2	G0IS.1	G0IS.0	00h
DBW0CON2	C5H	G0ASE	G0ARSEN	G0DBM.1	G0DBM.0	-	G0ASDSC	G0ASDSPPS	G0ADOEN	00h
DBW1CON1	C6H	G1ASDLB1	G1ASDLB0	G1ASDLA1	G1ASDLA0	G1IS.3	G1IS.2	G1IS.1	G1IS.0	00h
DBW1CON2	C7H	G1ASE	G1ARSEN	G1DBM.1	G1DBM.0	-	G1ASDSC	G1ASDSPPS	G1ADOEN	00h
DBW2CON0	BBH	-	-	-	-	G2EN	G2POLB	G2POLA	G2CS0	00h
DBW2CON1	BCH	G2ASDLB1	G2ASDLB0	G2ASDLA1	G2ASDLA0	G2IS.3	G2IS.2	G2IS.1	G2IS.0	00h
DBW2CON2	BDH	G2ASE	G2ARSEN	G2DBM.1	G2DBM.0	-	G2ASDSC	G2ASDSPPS	G2ADOEN	00h
BEEPER Register										
BEEPER	91H	BEEPEN	BEEPSEL.1	BEEPSEL.0	BEEPDIV.4	BEEPDIV.3	BEEPDIV.2	BEEPDIV.1	BEEPDIV.0	1Fh
AUX Control										
AUXCON	E8H	-	-	-	-	S003_SOPT	-	-	-	00h

7.3 Special Function Registers Definition

7.3.1 Accumulator – ACC

Table 7-4 ACC Register (E0h)

Bit	Symbol	Description	Type	Reset
acc.7~0	-	Accumulator	R/W	00h

Accumulator is used by most of the ET8051 instructions to hold the operand and to store the result of an operation. The mnemonics for accumulator-specific instructions refer to accumulator as A, not ACC.

7.3.2B Register – B

Table 7-5 B Register (F0h)

Bit	Symbol	Description	Type	Reset
b.7~0	-	B register for multiplying and division instructions	R/W	00h

The B register is used during multiplying and division instructions. It can also be used as a scratch-pad register to hold temporary data.

7.3.3Program Status Word Register - PSW

The PSW register contains status bits that reflect the current state of the CPU.

Note that the Parity bit can only be modified by hardware upon the state of ACC register.

Table 7-6 PSW Register (D0h)

Bit	Symbol	Description	Type	Reset
psw.7	cy	**Carry flag** Carry bit in arithmetic operations and accumulator for Boolean operations.	R/W	0
psw.6	ac	**Auxiliary Carry flag** Set if there is a carry-out from 3rd bit of Accumulator in BCD operations	R/W	0
psw.5	f0	**General purpose Flag 0** General purpose flag available for user	R/W	0
psw.4	rs1	**Register bank select** control bit 1, used to select working register bank	R/W	0
psw.3	rs0	**Register bank select** control bit 0, used to select working register bank	R/W	0
psw.2	ov	**Overflow flag** Set in case of overflow in Accumulator during arithmetic operations	R/W	0
psw.1	f1	**General purpose Flag 1** General purpose flag available for user	R/W	0
psw.0	p	**Parity flag** Reflects the number of '1's in the Accumulator P = '1' if Accumulator contains an odd number of '1's P = '0' if Accumulator contains an even number of '1's	R	0

The state of rs1 and rs0 bits selects the working register bank as follows:

Table 7-7 Register Bank Locations

rs1	rs0	Selected Register Bank	Location
0	0	Bank 0	(00H – 07H)

rs1	rs0	Selected Register Bank	Location
0	1	Bank 1	(08H – 0FH)
1	0	Bank 2	(10H – 17H)
1	1	Bank 3	(18H – 1FH)

7.3.4Stack Pointer - SP

Table 7-8 SP Register (81h)

Bit	Symbol	Description	Type	Reset
sp.7~0	-	Stack address	R/W	07h

This register points to the top of stack in internal data memory space.

It is used to store the return address of program before executing interrupt routine or subprograms. The SP is incremented before executing PUSH or CALL instruction and it is decremented after executing POP or RET(I) instruction (it always points the top of stack).

7.3.5Data Pointer – DPH, DPL

Table 7-9 DPL Register (82h)

Bit	Symbol	Description	Type	Reset
dpl.7~0	-	Data pointer low address	R/W	00h

Table 7-10 DPH Register (83h)

Bit	Symbol	Description	Type	Reset
dph.7~0	-	Data pointer high address	R/W	00h

Data Pointer Register can be accessed through DPL and DPH.

These registers are intended to hold 16-bit address in the indirect addressing mode used by MOVX (move external memory), MOVC (move program memory) or JMP (computed branch) instructions. They may be manipulated as 16-bit register or as two separate 8-bit registers. DPH holds higher byte and DPL holds lower byte of indirect address.

It is generally used to access external code or data space (e.g. MOVC A,@A+DPTR or MOV A,@DPTR respectively).

7.3.6Clock Control Register – CKCON

The contents of this register define the number of internally generated wait states that occur during read/write accesses to external data and program memory. It also controls the type of write access to either of the memory spaces.

The CKCON register is allocated in the SFR memory space when internal wait state generation is selected.

Table 7-11 CKCON Register (8Eh)

Bit	Symbol	Description	Type	Reset
ckcon.7	-	-	R	1
ckcon.6	-	Program memory wait state control	R/W	0
ckcon.5	-			0
ckcon.4	-			0
ckcon.3	-	-	R	1
ckcon.2	-	External data memory stretch cycle control	R/W	0
ckcon.1	-			0
ckcon.0	-			0

7.3.7Timed Access Register – TA

Table 7-12 TA Register (FFh)

Bit	Symbol	Description	Type	Reset
TA.7~0	-	The Timed Access register: The Timed Access register controls the access to protected bits. To access protected bits, the user must first write AAH to the TA. This must be immediately followed by a write of 55H to TA. Now a window is opened in the protected bits for three machine cycles, during which the user can write to these bits	W	FFh

The device has a new feature, like the Watchdog Timer which is a crucial to proper operation of the system. If left unprotected, errant code may write to the Watchdog control bits resulting in incorrect operation and loss of control. In order to prevent this, the device has a protection scheme which controls the write access to critical bits. This protection scheme is done using a timed access.

In this method, the bits which are to be protected have a timed write enable window. A write is successful only if this window is active, otherwise the write will be discarded. This write enable window is open for 3 machine cycles if certain conditions are met. After 3 machine cycles, this window automatically closes. The window is opened by writing AAh and immediately 55h to the Timed Access (TA) SFR. This SFR is located at address FFh. The suggested code for opening the

timed access window is

```
TA   REG    0FFh          ;Define new register TA, located at 0FFh
     MOV    TA,    #0AAh
     MOV    TA,    #055h
```

When the software writes AAh to the TA SFR, a counter is started. This counter waits for 3 machine cycles looking for a write of 55h to TA. If the second write (55h) occurs within 3 machine cycles of the first write (AAh), then the timed access window is opened. It remains open for 3 machine cycles, during which the user may write to the protected bits. Once the window closes the procedure must be repeated to access the other protected bits.

Examples of Timed Assessing are shown below.

Example:

```
MOV     TA,         #0AAh
MOV     TA,         #055h
MOV     WDTCON,     #00h
```

7.3.8 SRST

Table 7-13 SRST egister (F7h)

Bit	Symbol	Description	Type	Reset
srst.7~1	-	Reserved, should be read as 0	R/W	00h
srst.0	srst	Continuously set this bit twice involves a soft reset action, PC pointer will be reset to 0x0000, and SFR register will be reset to its reset value.	R/W	0

8 Enhanced CPU

The ET8051 is a high performance, opcode compatible core version of the industry standard 8051 micro controller.

It provides software and hardware interrupts, interfaces for serial communication, timer system with compare-capture-reload resources, extended multiplication-division unit, multi-purpose I/O ports, watchdog timer and debugger interface.

The architecture eliminates redundant bus states and implements parallel execution of fetch and execution phases. Since a cycle is aligned with memory fetch when possible, most of the 1-byte instructions are performed in a single cycle. The ET8051 uses 1 clock per cycle.

9 System Clock

9.1 Overview

The chip has a single system clock that is generated directly from one of four selectable clock sources: on-chip crystal oscillator, on-chip ceramic resonator, internal 4/8/12 MHz RC oscillator and external clock source. The clock source is selected by the code configuration words. The choice of clock source also affects the start-up time after a POR, LVR or STOP event.

In addition to this system clock, internal 32 KHz RC oscillator is used for WDT and time-out delay when power on reset.

The warm-up time is configured to maximum value to ensure that user can select all expected clock source.

9.2 Clock Definition

Symbol	Description
clk_osc	**Main oscillator** Four selectable clock sources: on-chip crystal oscillator, on-chip ceramic resonator, internal 4/8/12 MHz RC oscillator and external clock source. The clock source is selected by the code configuration words.
clk_32k	**Sub-oscillator** Internal 32 KHz RC oscillator is used for WDT and time-out delay when power on reset.
clk_sys	**System clock** The system clock is generated from the prescaler clock of clk_osc.
clk_cpu	**CPU clock** The CPU clock is generated from clk_sys.
clk_per	**Periphery clock** The periphery clock is generated from clk_sys.

Clock scheme within the system could see as below figure:

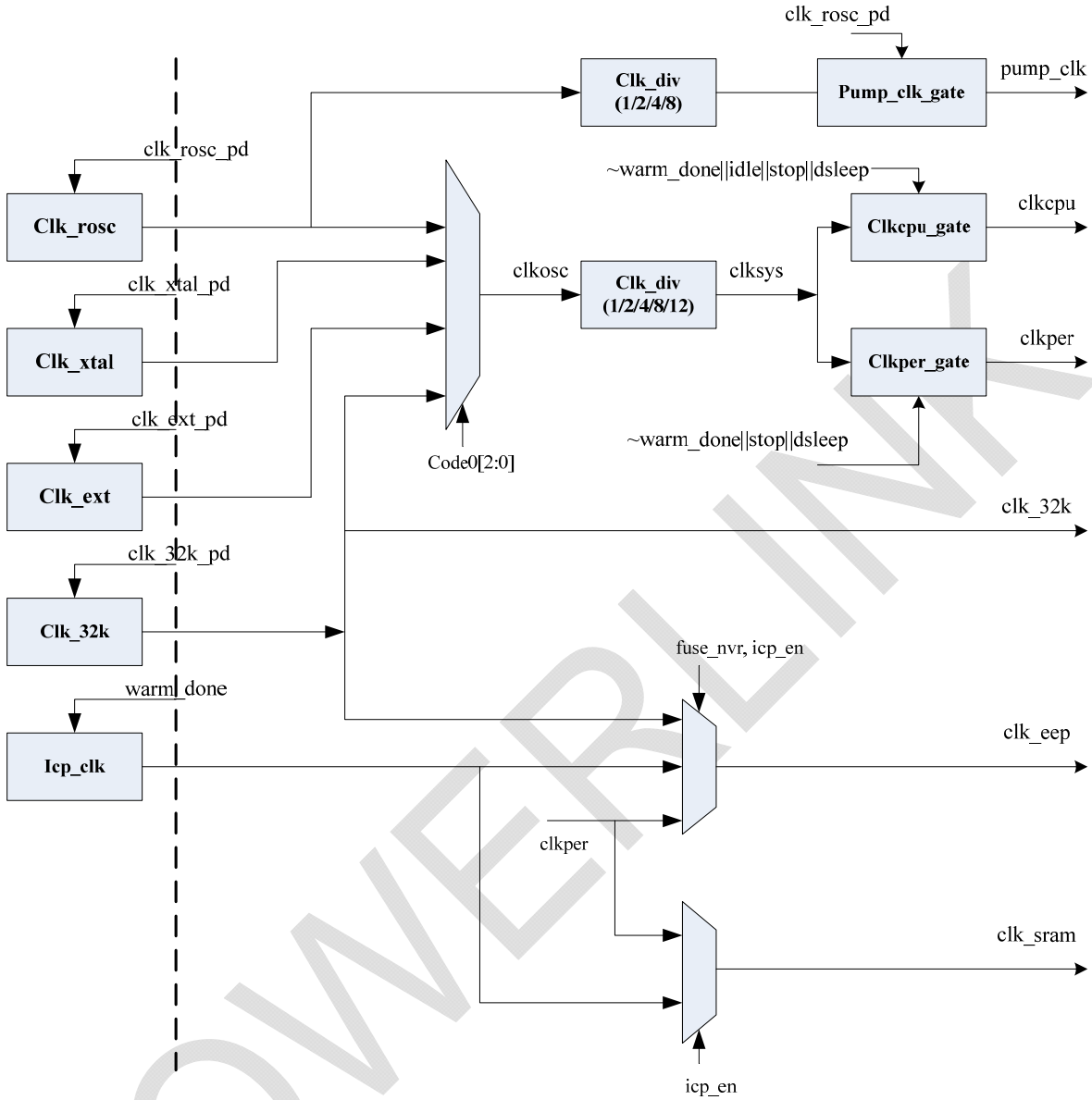


Figure 9-1 System Clock Scheme

Note:

1. clkcpu is gated when system enters into the idle/stop/sleep mode;
2. clkper is gated when system enters into the stop/sleep mode;

9.3 Crystal Oscillator and Ceramic Resonator

When enabled, internal inverting oscillator amplifier is connected between XIN and XOUT for connection to an external quartz crystal or ceramic resonator. The oscillator may operate in either high-speed or low-power mode. When the crystal frequency is less than 4MHz, the power

consumption of the chip is much smaller than that of the high speed mode, that is the low power mode.

An on-chip feedback resistor can be configured and connected between XIN and XOUT (the chip automatically adapts the appropriate on-chip feedback resistance value according to the crystal configuration word); In addition, two optional 15pF on-chip capacitors can be selected to connect between XIN/XOUT and GND. Those resistor and capacitors can improve the startup characteristics of the oscillator especially at higher frequencies. The resistor and capacitors can be configured with the config options.

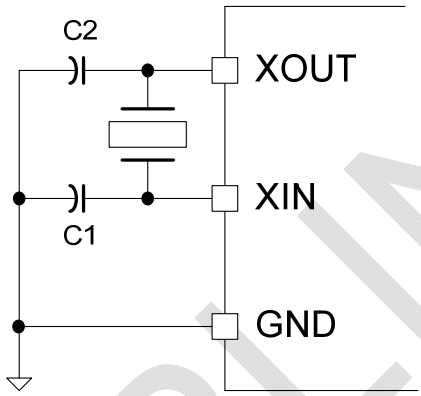


Figure 9-2 Crystal Oscillator and Ceramic Resonator

Note: C1, C2 = 0~15pF

9.4 Internal 4/8/12MHz RC Oscillator

A high accuracy internal 4/8/12MHz RC oscillator is integrated and calibrated with trimming config options.

Because EEPROM program will use the internal RC oscillator, it is always running when EEPROM is programming. When device start EEPROM program and then enter into STOP mode, the internal RC oscillator will not be disabled until EEPROM program is finished.

9.5 External Clock

When external clock source is selected by the config options, the external clock will be input from XIN. XOUT will be used for other pin functions.

9.6 Internal 32KHz RC Oscillator

The internal 32KHz RC oscillator is used for time-out delay time and WDT. When both WDT code fuse option is valid and WDTCON.WDTEN is set, it will run even device enter into STOP mode.

9.7 System Clock Output

When enable the oscillator clock out, the system clock can be output from P0.2. It will always output 1 during STOP mode.

9.8 Register Definition

9.8.1System Clock Prescaler Register - SCKCON

Table 9-1 SCKCON Register (96h)

Bit	Symbol	Description	Type	Reset
sckcon.7	-	**Interrupt mask while TA protects windows enable**	R/TW	0
sckcon.6		**SOSCSW clock source switch enable** 0 – Disable write SCKCON[5:4] 1 – Enable write SCKCON[5:4]	R/TW	0
sckcon.5		**TKC detection accelerate** 0 – Default TKC detection speed 1 – Accelerate TKC detection speed Note: SCKCON[5] can be modified only when SCKCON[6] is 1.	R/TW	0
sckcon.4	-	Reserved Note: just used for internal test, when using keep in 0	R/TW	0
sckcon.3	-	**System clock prescaler bits**	R/TW	0
sckcon.2	-			0
sckcon.1	-			0
sckcon.0	-			0

The base peripheral clock is the same as the CPU clock. It is affected by the prescaler. However, individual peripherals can have their clock further modified using the prescaler in the SCKCON register. The prescaler is a 4-bit prescaler controlled by the SCKCON.

Table 9-2 System Clock Prescaler

sckcon.3	sckcon.2	sckcon.1	sckcon.0	Prescaler		sckcon.3	sckcon.2	sckcon.1	sckcon.0	Prescaler
0	0	0	0	1		1	0	0	0	24
0	0	0	1	2		1	0	0	1	32
0	0	1	0	3		1	0	1	0	48
0	0	1	1	4		1	0	1	1	64
0	1	0	0	6		1	1	0	0	96

sckcon.3	sckcon.2	sckcon.1	sckcon.0	Prescaler		sckcon.3	sckcon.2	sckcon.1	sckcon.0	Prescaler
0	1	0	1	8		1	1	0	1	128
0	1	1	0	12		1	1	1	0	256
0	1	1	1	16		1	1	1	1	512

10 Reset

10.1 Overview

During reset, all I/O Registers are set to their initial values, the port pins are set to their default mode, and the program starts execution from the Reset Vector, 0000H. The device has four sources of reset: power-on reset, low voltage reset, external reset, hardware watchdog reset.

10.2 Power-on Reset

A Power-on Reset (POR) is generated by an on-chip detection circuit. The POR detection level is nominally 1.2V (Typ.). The BOR is activated whenever VDD is below 0.8V. The POR circuit can be used to trigger the start-up reset or to detect a major supply voltage failure. The POR circuit ensures that the device is reset from power-on.

When VDD reaches the Power-on Reset threshold voltage, the start-up time delay determines how long the device is kept in POR after VDD rise. The POR signal is activated again, without any delay, when VDD falls below the POR threshold level. A Power-on Reset (i.e. a cold reset) will set the PORF flag in RSTCON. The internally generated reset can be extended beyond the power-on period by holding the RST pin active longer than the time-out.

The start-up time delay is user-configurable with the start-up time fuses and depends on the clock source. The start-up time fuses also control the length of the start-up time after a Brown-out Reset or when waking up from Power-down during internally timed mode. The start-up delay should be selected to provide enough settling time for VDD and the selected clock source. The device operating environment (supply voltage, frequency, temperature, etc.) must meet the minimum system requirements before the device exits reset and starts normal operation.

Table 10-1 Time-out Delay Settings

Time-out Option (CODE1.TOUT)	Time-out Clock	Time-out Delay
		32K
00	(16ms+4 *4ms retry) * 2	64 ms
01	(16ms+4 *4ms retry) + 512(clk32k)	48 ms
10	(16ms+4 *4ms retry) + 256(clk32k)	40 ms
11	(16ms+4 *4ms retry) + 4(clk32k)	32 ms

Table 10-2 Warm-up Time Settings

Clock Source	Warm-up Time (CODE1.WARM)			
	00	01	10	11

Clock Source	Warm-up Time (CODE1.WARM)			
	00	01	10	11
Crystal Oscillator/Ceramic Resonator	2048 Clocks	1024 Clocks	256 Clocks	64 Clocks
Internal RC Oscillator	1024 Clocks	256 Clocks	64 Clocks	8 Clocks
External Clock	64 Clocks	8 Clocks	0 Clocks	0 Clocks

The start-up time delay includes both time-out delay and the warm-up time when device starts up from reset. When device starts up from STOP mode, only warm-up time is needed.

The RST pin may be held active externally until these conditions are met.

10.3 Low Voltage Reset

The device has an on-chip low voltage reset (LVR) circuit for monitoring the VDD level during operation by comparing it to a fixed trigger level.

A hysteresis of trigger level is designed to prevent LVR from spike. When VDD decreases to a value below the trigger level V_{LVT}, the internal reset is immediately activated. When VDD increases above the trigger level plus about V_{HYST} of hysteresis, the device releases the internal reset after the specified time-out period has expired.

The LVR does not generate a reset output pulse except as part of a POR event.

A low voltage reset will set the LVRF flag in RSTCON.

10.4 Low Power Detect

The device has an on-chip low power detect (LPD) circuit for monitoring the VDD level during operation by comparing it to a fixed trigger level. The trigger level for the LPD is selected by config options. The purpose of the LPD is to ensure that if VDD fails or dips while executing at speed, the system will gracefully enter reset without the possibility of errors induced by incorrect execution.

The LPD does not generate a reset, it will only set the LPDF flag in RSTCON.

10.5 External Reset

The RSTB pin can function as either an active-low reset input. Entry into reset is completely asynchronous. The presence of the active reset level on the input will immediately reset the device. A glitch filter will suppress all reset input pulses of less than 50 ns. Exit from reset is synchronous. In Compatibility mode the reset pin is sampled every six clock cycles and must be held inactive for at least twelve clock cycles to deassert the internal reset. In Fast mode the reset pin is sampled every clock cycle and must be held inactive for at least two clock cycles to deassert the internal reset.

The device includes an on-chip Power-On Reset and Low Voltage Reset circuit that ensures that the device is reset from system power up. In most cases a RC startup circuit is not required on the RSTB

pin, reducing system cost, and the RSTB pin may be left unconnected if a board-level reset is not present.

A external reset will set the EXRF flag in RSTCON.

10.6 Hardware Watchdog Reset

When the hardware watchdog times out, it will generate a reset pulse lasting 16 clock cycles. The WDT can be enabled by config options.

A hardware watchdog reset will set the WDRF flag in RSTCON.

10.7 Register Definition

10.7.1 Reset Control Register - RSTCON

Table 10-3 RSTCON Register (F8h)

Bit	Symbol	Description	Type	Reset
rstcon.7~6	-	-	R	00b
rstcon.5	-	-	R	1
rstcon.4	LPDF	**Low Power Detect Flag** This bit is set to 1 by hardware when a LPD is active. And it can only be cleared by software or POR	R/W	0
rstcon.3	PORF	**Power-on Reset Flag** This bit is set to 1 by hardware when a POR is active. And it can only be cleared by software.	R/W	1
rstcon.2	LVRF	**Low Voltage Reset Flag** This bit is set to 1 by hardware when a LVR is active. And it can only be cleared by POR or software.	R/W	0
rstcon.1	EXRF	**External Reset Flag** This bit is set to 1 by hardware when an external reset is active. And it can only be cleared by POR or software.	R/W	0
rstcon.0	WDRF	**Watchdog Reset Flag** This bit is set to 1 by hardware when a WDT reset is active. And it can only be cleared by POR or software. Read or write this bit can clear hardware watchdog timer if WDT is enabled.	R/W	0

Note: In normal mode, after power-on, read rstcon.5 the value must be 1, otherwise the system can not work. The ’rstcon.2’ and ’rstcon.1’ perhaps read out as 1’b1 when LVR/EXT_RST are enabled in CODE configuration, that means these resets happened once, clear these flags before using the flag is recomendded.

11 Power Saving Modes

11.1 Overview

The device supports three different software selectable power-reducing modes: IDLE, STOP and SLEEP. These modes are accessed through the PCON register.

Table 11-1 Power Saving Mode Type

PSW types / PSW blocks		IDLE		STOP		SLEEP	
		Clock	Power	Clock	Power	Clock*(1)	Power*(1)
Digital	CPU core	off	on	off	on	off	off
	Peripheral	on	on	off	on	off	off
Memory	EEPROM	on*(2)	on	off	on	off	off
	IRAM	off	on	off	on	off	off
Analog	Power supply	-	on	-	on	-	off
	IRC4/8/12Mhz	on	on	off	off	off	off
	IRC32Khz	on	on	off	off	off	off
	Oscillator	on	on	off	off	off	off
	ACMP	-	acmpcon0[6]	-	acmpcon0[6]	-	acmpcon0[6]
	ADC	on	on	on	on	on	on

Note:

1. Power supply is about 1.5v (w/ 32K LIRC) or 1.2v (w/o 32K LIRC) in SLEEP mode, for Internal SRAM retention, and not be powered off actually.
2. The clock of EEPROM could be active even if 'cpuclk' is turnoff in IDLE mode;

11.2 IDLE Mode

Setting the IDLE bit in PCON enters IDLE mode. IDLE mode halts the internal CPU clock. The CPU state is preserved in its entirety, including the RAM, stack pointer, program counter, program status word, and accumulator. The Port pins hold the logic states they had at the time that IDLE was activated. IDLE mode leaves the peripherals running in order to allow them to wake up the CPU when an interrupt is generated. The timer and UART peripherals continue to function during IDLE. If these functions are not needed during IDLE, they should be explicitly disabled by clearing the appropriate control bits in their respective SFRs. The Low Voltage Reset is always active during IDLE.

Any enabled interrupt source or reset may terminate IDLE mode. When exiting IDLE mode with an interrupt, the interrupt will immediately be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into IDLE.

The power consumption during IDLE mode can be further reduced by prescaling down the system clock using the System Clock Prescaler. Be aware that the clock divider will affect all peripheral functions and baud rates may need to be adjusted to maintain their rate with the new clock frequency.

11.3 STOP Mode

Setting the STOP bit in PCON enters STOP mode. STOP mode stops the oscillator, disables the LVR and powers down the Flash memory in order to minimize power consumption. Only the power-on circuitry will continue to draw power during STOP. During STOP, the power supply voltage may be reduced to the RAM keep-alive voltage. The RAM contents will be retained, but the SFR contents are not guaranteed once VDD has been reduced. STOP could be exited by external reset, power-on reset, LVR reset, WDT reset or certain enabled interrupts.

Six enabled external interrupt sources could be configured to wakeup STOP mode directly: external interrupts INT0B and INT1B (only support level-activated), keyboard interrupt, analog comparator interrupt, touch key interrupt，WDT interrupt. When exiting STOP mode with an interrupt, the interrupt will immediately be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into STOP.

Note:

1) If set STOP and IDLE bits simultaneously, device will enters STOP mode. When device is waked up from STOP mode, both STOP and IDLE bits will be cleared by hardware.
2) To wake up from STOP mode, the enabled external interrupts must be active long enough for start-up time delay.
3) To wake up from STOP mode, RSTB pin must be active long enough for start-up time delay.

11.4 SLEEP Mode

Setting the SLEEP bit in PCON enters SLEEP mode. In SLEEP mode, reduced power supply of 1.5v to 1.2v (w/o 32K LIRC) more or less, in order to minimize power consumption but still keeping the contents stored in the IRAM, also all the other analog circuit including the Flash memory and the oscillators and Internal RC are also powered off, shut down CPU clock and the peripheral’s clock.

When system entered into SLEEP mode, external interrupts INT0B and INT1B, WDT interrupt, keyboard interrupt or touch key interrupt could wakeup system directly when they are enabled, and run program from the interrupt point after the system is return. Four types of reset including POR reset, LVR reset WDT reset or external reset will reset the system and run program from the start PC value.

11.5 Register Definition

11.5.1 Power Control Register - PCON

Table 11-2 PCON Register (87h)

Bit	Symbol	Description	Type	Reset
pcon.7	PGSEL1	**XDATA 8-bit Page select** 00：0x0000~0x00FF 01：0x0100~0x01FF 10：0x0200~0x02FF 11：0x0300~0x03FF	-/TW	0
pcon.6	PGSEL0			
pcon.5	ISR_TM	**Interrupt Service Routine Test Mode flag** When set to 1, the interrupt vectors assigned to Timer 0 & 1, Serial Port 0 & 1, SPI and I2C interfaces can be triggered only with the use of external inputs of the core	R/TW	0
pcon.4	PMW	**Program memory write mode** 1: Setting this bit enables the program memory write mode	R/TW	0
pcon.3	P2SEL	**High-order address byte configuration bit** Chooses the higher byte of address (“memaddr[15:8]”) during MOVX @Ri operations; 1：“memaddr[15:8]” = {6’b0, PGSEL[1:0]} 0：“memaddr[15:8]” = P2reg	R/TW	1
pcon.2	SLEEP	**SLEEP mode control** Setting this bit will auto-set STOP (pcon.1) bit, and let chip go into SLEEP mode. This bit is always read as 0	R/TW	0
pcon.1	STOP	**STOP mode control** Setting this bit activates STOP mode. This bit is always read as 0	R/W	0
pcon.0	IDLE	**IDLE mode control** Setting this bit activates IDLE mode. This bit is always read as 0	R/W	0

12 Interrupts

12.1 Overview

The chip adopts four interrupt priority structure, which provides great flexibility for multi-interrupt source processing. The chip supports 16 interrupt sources,(each interrupt source has its own priority control bit, flag bit, interrupt vector, interrupt enable bit. In addition, these interrupts can be independently enabled or disabled globally.)Each interrupt source can be independently enabled or disabled by setting or clearing the corresponding bits in IEN0 and IEN1. IEN0 also contains a global stop bit EA, which disable all interrupts.

Each interrupt source can be individually priorities by clearing or setting the corresponding bits in IP0, IP0H, IP1 and IP1H, respectively. An interrupt service routine can be interrupted at a higher priority, but not at the same or lower priority. The highest level interrupt service routine does not respond to any other interrupt. If two interrupt sources with different interrupt priorities request interrupt at the same time at the start of the instruction, the interrupt request with higher priority is responded.

If two interrupt sources of the same priority request an interrupt at the same time as the instruction begin, an internal query sequence determines which interrupt request to respond to first. This is called the quorum queue. Note: The quorum queue is only used to process interrupt sources of the same priority and apply for an interrupt at the same time.

12.2 Interrupt Sources

The External Interrupts INT0B and INT1B can be either edge triggered or level triggered, depending on bits IT0 and IT1. The bits IE0 and IE1 in the TCON register are the flags which are checked to generate the interrupt. In the edge triggered mode, the INTx inputs are sampled in every machine cycle. If the sample is high in one cycle and low in the next, then a high to low transition is detected and the interrupts request flag IEx in TCON is set. The flag bit requests the interrupt. Since the external interrupts are sampled every machine cycle, they have to be held high or low for at least one complete machine cycle.

The IFx flag is automatically cleared when the service routine is called.

If the level triggered mode is selected, then the requesting source has to hold the pin low till the interrupt is serviced. The IFx flag will not be cleared by the hardware on entering the service routine. If the interrupt continues to be held low even after the service routine is completed, then the processor may acknowledge another interrupt request from the same source.

The Timer 0, 1 and 2 Interrupts are generated by the TF0, TF1 and TF2 flags. These flags are set by the overflow in the Timer 0, Timer 1 and Timer 2. The TF0 and TF1 flags are automatically cleared by the hardware when the timer interrupt is serviced, TF2 flag should be cleared by software.

The Serial block can generate interrupt on reception or transmission. There are two interrupt sources

from the Serial block, which are obtained by the RI and TI bits in the SCON SFR. These bits are not automatically cleared by the hardware, and the user will have to clear these bits by software.

All the bits that generate interrupts can be set or reset by software, and thereby software initiated interrupts can be generated. Each of the individual interrupts can be enabled or disabled by setting or clearing a bit in the IEN0 and IEN1 SFR. IEN0 also has a global enable/disable bit EA, which can be cleared to disable all interrupts.

The EEPROM write finished can generate interrupt after finished EEPROM write operation. There is one interrupt source, which is obtained by the PGMF bit in the EECON SFR. This flag is automatically cleared by the hardware when the EEPROM program finish interrupt is serviced.

The analog comparator can generate interrupt after comparator output has toggle occurs by CMPF. This flag is automatically cleared by the hardware when the ACMP interrupt is serviced.

The keyboard can generate interrupt after keyboard output has toggle occurs by KBF. This bit is automatically cleared when pressed key is released.

The capsensor can generate interrupt after capsensor output has toggle occurs by TKF. This bit is not automatically cleared by the hardware, and the user will have to clear this bit using software.

The I2C function can generate interrupt, if EI2C and EA bits are enabled, when SI Flag is set due to a new I2C status code is generated, SI flag is generated by hardware and must be cleared by software.

The SPI function can generate interrupt, if ESPI and EA bits are enabled, when ‘spif’ flag is set due to a new 8-bit data frame transfer completion, the flag is generated by hardware and must be cleared by software.

The WDT function can generate interrupt，if WDTIEN and EA bits are enabled, when WDTIF flag is set due to WDT time overflow ,the flag is generated by hardware and automatically cleared by the hardware when the WDT interrupt is serviced.

The interrupt flags are sampled every machine cycle. In the same machine cycle, the sampled interrupts are polled and their priority is resolved. If certain conditions are met then the hardware will execute an internally generated LCALL instruction which will vector the process to the appropriate interrupt vector address. The conditions for generating the LCALL are;

1. An interrupt of equal or higher priority is not currently being serviced.
2. The current polling cycle is the last machine cycle of the instruction currently being execute.
3. The current instruction does not involve a write to IE, EIE, IP0, IP0H, IP1 or IPH1 registers and is not a RETI. In other words, an interrupt request is not immediately responded to after RETI or reading or writing IE, EIE, IP0, IP0H, IP1, or IPH1, at least until one other instruction is ececuted.

Note: Since it usually takes 2 instructions to change the priority is recommended that the appropriate interrupt be turned off during this time to avoid an interrupt during the priority change process. If the interrupt flag is no longer valid when the module state changes, this interrupt will not be responded to. Each period of the polling detects the valid interrupt request.

If any of these conditions are not met, then the LCALL will not be generated. The polling cycle is repeated every machine cycle, with the interrupts sampled in the same machine cycle. If an interrupt flag is active in one cycle but not responded to, and is not active when the above conditions are met, the denied interrupt will not be serviced. This means that active interrupts are not remembered; every polling cycle is new.

These address of vector for the different sources are as follows:

Table 12-1 Vector Locations for Interrupt Sources

Interrupt	Source	Vector	No.		Interrupt	Source	Vector	No.
System Reset	RST	0000H						
External Interrupt0	IE0	0003H	0		Timer0 Overflow	TF0	000BH	1
External Interrupt1	IE1	0013H	2		Timer1 Overflow	TF1	001BH	3
Serial Port Interrupt	RI or TI	0023H	4		Timer2 Overflow or External Reload	TF2	002BH	5
I2C Interrupt	I2CF	0033H	6		Keyboard Interrupt	KBF	003BH	7
SPI Interrupt	SPIF	0043H	8		ADC Interrupt	ADC	004BH	9
Timer2 Capture/Compare	T2CF	0053H	10		EE Write Finshed Interrupt	PGMF	005BH	11
Comparator Interrupt	CMPF	0063H	12		LPD interrupt	LPDF	006BH	13
Serial1 Port Interrupt	RI1 or TI1	0073H	14		WDT interrupt	WDTIF	007BH	15
Reserved		0083H	16		Reserved		008BH	17
Reserved		0093H	18		Reserved		009BH	19

The CPU responds to valid interrupts by invoking the interrupt service routine through LCALL, which pushed the contents of the program counter onto the stack (but does not hold the PSW) and then stores the vector address of the corresponding interrupt source into the program counter. The interrupt service starts at the specified address and end with the RETI instruction. The RETI instruction notifies the CPU that the interrupt service routine is over, pops the two bytes of the stack, reloads the interrupt service routine into the program counter and returns to where it left off. RETI instructions can also return to the original address to continue execution, but the interrupt priority control system still considers an interrupt of the same priority to be responded, in which case the same or lower priority will not be responded.

12.3 Priority Level Structure

The device uses a four priority level interrupt structure (highest, high, low and lowest) and supports up to 16 interrupt sources. The interrupt sources can be individually set to either high or low levels. Naturally, a higher priority interrupt cannot be interrupted by a lower priority interrupt. However there exists a pre-defined hierarchy amongst the interrupts themselves. This hierarchy comes into

play when the interrupt controller has to resolve simultaneous requests having the same priority level. This hierarchy is defined as table below. This allows great flexibility in controlling and handling many interrupt sources.

Table 12-2 Four-level Interrupt Priority

Priority Bits		Interrupt Level Priority
IPXH	IPX	
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the IP0, IP0H, IP1, and IP1H registers. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. So, if two requests of different priority levels are received simultaneously, the request of higher priority level is serviced.

If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve simultaneous requests of the same priority level.

As below Table summarizes the interrupt sources, flag bits, vector addresses, enable bits, priority bits, arbitration ranking, and whether each interrupt may wake up the CPU from STOP mode.

Table 12-3 Vector location for Interrupt sources and STOP mode Wakeup

Source	Flag	Vector Address	Interrupt Enable Bits	Interrupt Priority	Flag Cleard By	Arbitration Ranking	STOP mode Wake-up
System Reset	RST	0000H	/	/	Software	/	Yes
External Interrupt 0	IE0	0003H	EX0 (IE0.0)	IP0H.0, IP0.0	Hardware	1 (highest)	Yes
Timer0 Interrupt	TF0	000BH	ET0 (IE0.1)	IP0H.1, IP0.1	Hardware, Software	2	No
External Interrupt 1	IE1	0013H	EX1 (IE0.2)	IP0H.2, IP0.2	Hardware	3	Yes
Timer1 Interrupt	TF1	001BH	ET1 (IE0.3)	IP0H.3, IP0.3	Hardware, Software	4	No
Serial 0 Port Tx and Rx	TI0&RI0	0023H	ES0 (IE0.4)	IP0H.4, IP0.4	Software	5	No
Timer2 Overflow or External Reload	TF2	002BH	ET2(IE0.5)	IP0H.5, IP0.5	Software	6	No

Source	Flag	Vector Address	Interrupt Enable Bits	Interrupt Priority	Flag Cleard By	Arbitration Ranking	STOP mode Wake-up
I2C Interrupt	I2CF	0033H	EI2C (IE1.0)	IP1H.0, IP1.0	Software	7	No
Keyboard Interrupt	KBF	003BH	EKB (IE1.4)	IP1H.4, IP1.4	Hardware, Software	8	Yes
SPI Interrupt	SPIF	0043H	ESPI(IE1.1)	IP1H.1, IP1.1	Software	9	No
ADC Interrupt	ADCF	004BH	ETK(IE1.5)	IP1H.5, IP1.5	Hardware, Software	10	Yes
Timer2 Capture/Compare Interrupt	T2CF	0053H	ET2C(IE1.3)	IP1H.3, IP1.3	Hardware, Software	11	No
EE Write Finshed Interrupt	PGMF	005BH	EPGM (EECON.3)	IP0H.7, IP0.7	Hardware	12	No
Comparator Interrupt	CMPF	0063H	ECMP (IE1.2)	IP1H.2, IP1.2	Hardware, Software	13	Yes*
LPD interrupt	LPDF	006BH	ELPD (IE1.6)	IP1H.6, IP1.6	Hardware, Software	14	Yes*
Serial 1 Port Interrupt	RI1 or TI1	0073H	ES1 (IE0.6)	IP0H.6, IP0.6	Hardware, Software	15	Yes*
WDT Interrupt	WDTIF	007BH	EWDT (wdtcon.5)	IP1H.7, IP1.7	Hardware, Software	16 (lowest)	Yes*

Note:

* Only level interrupt generated from comparator could wakeup from STOP mode.

12.4 Response Time

The response time for each interrupt source depends on several factors, such as the nature of the interrupt and the instruction underway. For all of the 16 interrupt source signals, they are sampled at every system clock cycle and then their corresponding interrupt flags will be set or reset. These flag values are polled in the next cycle, and core responses it at the second cycle, interrupt spot is protect and ‘PC’ value is stored in the third cycle, then the interrupt vector is loaded into ‘PC’ in the forth cycle. So if an interrupt request is active and is selected as a active interrupt source according the configuration in SFR ‘IEx’, ‘IPx’, there is a minimum time of four system clock cycles between the interrupt flag being set and the interrupt service routine being executed.

A longer response time should be anticipated if any of the three conditions are not met. If a higher or equal priority is being serviced, then the interrupt latency time obviously depends on the nature of the service routine currently being executed.

12.5 Interrupt Inputs

The device has 16 interrupts source, they wire-OR together, and form one internal interrupt signal 'irq' connected to core. Only 6 of these input interrupts could be configured to wakeup the processor and resume operation when device is put into STOP or IDLE mode, they are INT0, INT1, touch key interrupt, keyboard interrupt, comparator interrupt, WDT interrupt.

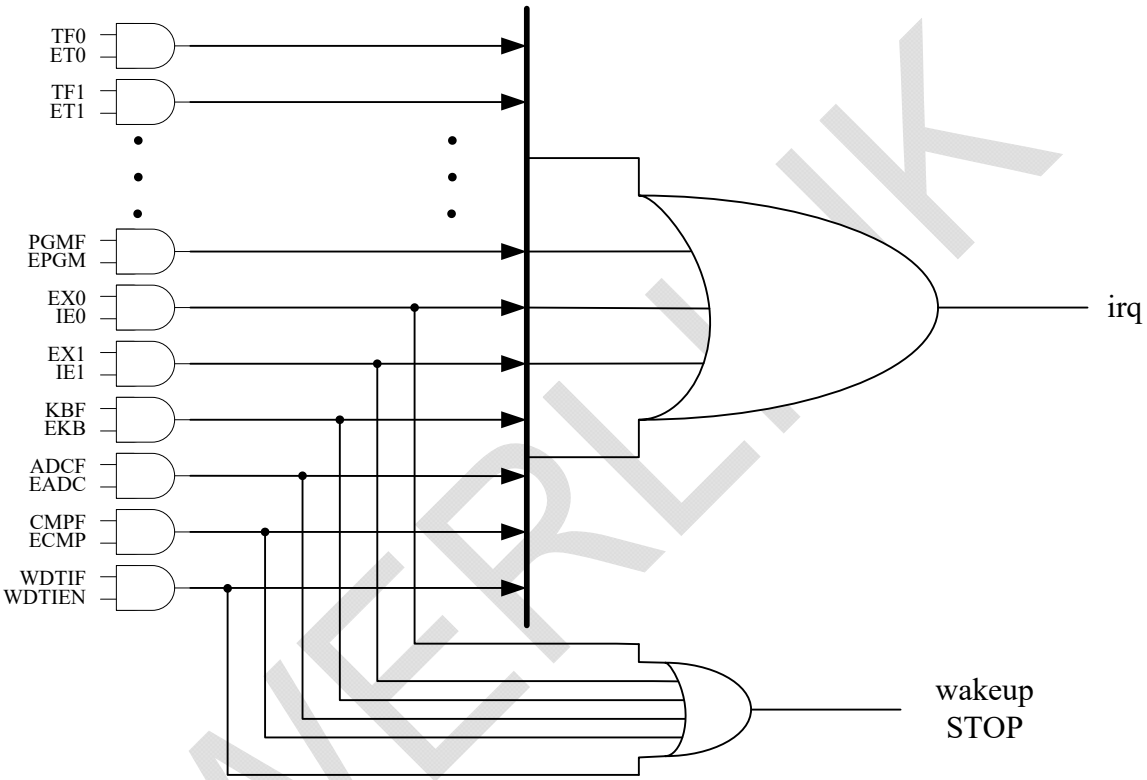


Figure 12-1 Interrupt IRQ and wakeup-STOP

Note:

1. 'irq' is interrupt signal to core, it could wakeup system when its in idle mode;
2. 'wakeup_stop' is used to wakeup system when its in stop mode;
3. 'wakeup_stop' could wakeup system when its in sleep mode;

12.6 Register Definition

12.6.1 Interrupt Enable 0 Register – IE0

Table 12-4 IE0 Register (A8h)

Bit	Symbol	Description	Type	Reset

Bit	Symbol	Description	Type	Reset
ie0.7	EA	**Interrupts enable** When set to 0 – all interrupts are disabled Otherwise enabling each interrupt is done by setting the corresponding interrupt enable bit	R/W	0
ie0.6	ES1	**Serial Port 1 interrupt enable** When es1=0 Serial Port 1 interrupt is disabled. When es1=1 and ea=1 Serial Port 1 interrupt is enabled.	R/W	0
ie0.5	ET2	**Timer2 interrupt enable** When et2=0 timer2 interrupt is disabled. When et2=1 and ea=1 timer2 interrupt is enabled.	R/W	0
ie0.4	ES0	**Serial Port 0 interrupt enable** When es0=0 Serial Port 0 interrupt is disabled. When es0=1 and ea=1 Serial Port 0 interrupt is enabled.	R/W	0
ie0.3	ET1	**Timer1 overflow interrupt enable** When et1=0 timer0 overflow interrupt is disabled. When et1=1 and ea=1 timer1 overflow interrupt is enabled.	R/W	0
ie0.2	EX1	**External interrupt 1 enable** When ex1=0 external interrupt 1 is disabled. When ex1=1 and ea=1 external interrupt 1 is enabled.	R/W	0
ie0.1	ET0	**Timer0 overflow interrupt enable** When et0=0 timer0 overflow interrupt is disabled. When et0=1 and ea=1 timer0 overflow interrupt is enabled.	R/W	0
ie0.0	EX0	**External interrupt 0 enable** When ex0=0 external interrupt 0 is disabled. When ex0=1 and ea=1 external interrupt 0 is enabled.	R/W	0

12.6.2 Interrupt Enable 1 Register – IE1

Table 12-5 IE1 Register (B8h)

Bit	Symbol	Description	Type	Reset
ie1.7	ET2R	**Timer2 external reload interrupt enable** When et2r=0, timer2 external reload interrupt is disabled. When et2r=1 and ea=1, timer2 external reload interrupt is enabled	R/W	0
ie1.6	ELPD	Low Power detect interrupt enable When elpd=0, low power detect interrupt is disabled When ea=1, elpd=1, low power detect interrupt is enabled	R/W	0
ie1.5	EADC	**ADC interrupt enable** When eadc=0 ADC interrupt is disabled.	R/W	0

Bit	Symbol	Description	Type	Reset
		When eadc=1 and ea=1 touch key interrupt is enabled.		
ie1.4	EKB	**Keyboard interrupt enable** When ekb=0 keyboard interrupt is disabled. When ekb=1 and ea=1 keyboard interrupt is enabled.	R/W	0
ie1.3	ET2C	**Timer2 capture and compare mode interrupt enable** When et2c=0, timer2 capture and compare interrupt is disabled. When et2c=1 and ea=1, timer2 capture and compare interrupt is enabled.	R/W	0
ie1.2	ECMP	**Analog comparator interrupt enable** When ecmp=0 comparator interrupt is disabled. When ecmp=1 and ea=1 comparator interrupt is enabled.	R/W	0
ie1.1	ESPI	**SPI interrupt enable** When espi=0 SPI interrupt is disabled. When espi=1 and ea=1 SPI interrupt is enabled.	R/W	0
ie1.0	EI2C	**I2C interrupt enable** When ei2c=0 I2C interrupt is disabled. When ei2c=1 and ea=1 I2C interrupt is enabled.	R/W	0

12.6.3 Interrupt Request Control Register - IRCON

Table 12-6 IRCON Register (C0h)

Bit	Symbol	Description	Type	Reset
ircon.7	T2RF	Timer 2 external reload flag software clear	R/W	0
ircon.6	TF2	Timer 2 overflow flag software clear	R/W	0
ircon.5	ADCF	ADC interrupt flag Interrupt ack Hard self-clear, software clear	R/W	0
ircon.4	KBF	Keyboard interrupt flag Interrupt disappear Hard self-clear ,software clear	R/W	0
ircon.3	T2CF	Timer2 capture and compare mode interrupt flag Interrupt ack Hard self-clear, software clear	R/W	0
ircon.2	CMPF	Analog comparator interrupt flag Interrupt ack Hard self-clear, software clear	R/W	0
ircon.1	-	-	R	0
ircon.0	-	-	R	0

12.6.4 Interrupt Priority 0 Register – IP0

Table 12-7 IP0 Register (A9h)

Bit	Symbol	Description	Type	Reset
ip0.7	PEEL	EEPROM write finished interrupt priority	R/W	0
ip0.6	PS1L	Serial Port 1 interrupt priority	R/W	0
ip0.5	PT2L	Timer2 interrupt priority	R/W	0
ip0.4	PS0L	Serial Port 0 interrupt priority	R/W	0
ip0.3	PT1L	Timer1 overflow interrupt priority	R/W	0
ip0.2	PX1L	External interrupt 1 priority	R/W	0
ip0.1	PT0L	Timer0 overflow interrupt priority	R/W	0
ip0.0	PX0L	External interrupt 0 priority	R/W	0

12.6.5 Interrupt High Priority 0 Register – IP0H

Table 12-8 IP0H Register (AAh)

Bit	Symbol	Description	Type	Reset
ip0h.7	PEEH	EEPROM write finished interrupt high priority	R/W	0
ip0h.6	PS1H	Serial Port 1 interrupt high priority	R/W	0
ip0h.5	PT2H	Timer2 interrupt high priority	R/W	0
ip0h.4	PS0H	Serial Port 0 interrupt high priority	R/W	0
ip0h.3	PT1H	Timer1 overflow interrupt high priority	R/W	0
ip0h.2	PX1H	External interrupt 1 high priority	R/W	0
ip0h.1	PT0H	Timer0 overflow interrupt high priority	R/W	0
ip0h.0	PX0H	External interrupt 0 high priority	R/W	0

12.6.6 Interrupt Priority 1 Register – IP1

Table 12-9 IP1 Register (B9h)

Bit	Symbol	Description	Type	Reset
ip1.7	PWDTL	WDT interrupt priority	R/W	0
ip1.6	PLPDL	Low Power Detect priority	R/W	0
ip1.5	PADCL	ADC interrupt priority	R/W	0
ip1.4	PKBL	Keyboard interrupt priority	R/W	0
ip1.3	PT2CL	Timer2 capture and compare mode interrupt priority	R/W	0

Bit	Symbol	Description	Type	Reset
ip1.2	PCMPL	Analog comparator interrupt priority	R/W	0
ip1.1	PSPIL	SPI interrupt priority	R/W	0
ip1.0	PI2CL	I2C interrupt priority	R/W	0

12.6.7 Interrupt High Priority 1 Register – IP1H

Table 12-10 IP1H Register (BAh)

Bit	Symbol	Description	Type	Reset
ip1h.7	PWDTH	WDT interrupt high priority	R/W	0
ip1h.6	PLPDH	Low Power Detect high priority	R/W	0
ip1h.5	PADCH	ADC interrupt high priority	R/W	0
ip1h.4	PKBH	Keyboard interrupt high priority	R/W	0
ip1h.3	PT2CH	Timer2 capture and compare mode interrupt high priority	R/W	0
ip1h.2	PCMPH	Analog comparator interrupt high priority	R/W	0
ip1h.1	PSPIH	SPI interrupt high priority	R/W	0
ip1h.0	PI2CH	I2C interrupt high priority	R/W	0

13 External Interrupts

The INT0B and INT1B pins of the device may be used as external interrupt sources. The external interrupts can be programmed to be level-activated or transition activated by setting or clearing bit IT1 or IT0 in Register TCON. If ITx = 0, external interrupt INTx is triggered by a detected low at the INTx pin. If ITx = 1, external interrupt INTx is falling edge-triggered. In this mode if successive samples of the INTx pin show a high in one cycle and a low in the next cycle, interrupt request flag IEx in TCON is set. Flag bit IEx then requests the interrupt.

Since the external interrupt pins are sampled once each clock cycle, an input high or low should hold for at least 2 system periods to ensure sampling. If the external interrupt is transition-activated, the external source has to hold the request pin high for at least two clock cycles, and then hold it low for at least two clock cycles to ensure that the transition is seen so that interrupt request flag IEx will be set. IEx will be automatically cleared by the CPU when the service routine is called if generated in edge-triggered mode.

If the external interrupt is level-activated, the external source has to hold the request active until the requested interrupt is actually generated. Then the external source must deactivate the request before the interrupt service routine is completed, or else another interrupt will be generated. Both INT0 and INT1 may wake up the device from the Power-down state.

By default, external interrupts INT0B and INT1B (level valid only) can wake up the chip from STOP and SLEEP modes.

When it is necessary to wake up STOP, SLEEP by external interrupt edge (rising edge, falling edge, double edge), the register must be set to internal low level trigger, and select the desired edge mode in the configuration word:

External interrupts trigger supplementary mode release mode selection bits.	**External interrupt X triggers supplementary mode selection bit**
0- Released by Ifx 1- Released by intxack	00–default mode, controlled by itx&itx_inv 01–Posedge trigger(internal low level trigger) 10–Negedge trigger(internal low level trigger) 11–Double edge trigger(internal low level trigger)

14 Keyboard Interface

The device implements a keyboard interface allowing the connection of a 1 x n to 8 x n matrix keyboard. The keyboard function provides 8 configurable external interrupts, each key reuse with port1.0~port1.7.

When an interrupt condition on a pin is detected, and that pin is enabled in the keyboard control register (KBCON), the keyboard interrupt flag (KBF) is set. The KBF flag will be automatically cleared when pressed key is released. Any enabled keyboard interrupt may wake up the device from the IDLE, STOP or SLEEP mode.

User need to poll the keyboard pins to detect which key input is active.

14.1 Register Definition

14.1.1 Keyboard Interrupt Control Register – KBCON

Table 14-1 KBCON Register (A7h)

Bit	Symbol	Description	Type	Reset
kbcon.7~0	-	Keyboard Interrupt control bits	R/W	00h

15 I/O Ports

15.1 Overview

The device has three I/O ports, port 0, port 1 and port 2. All pins of I/O ports can be configured by config options and port control registers. Maximal 22 general purpose I/O ports can be set.

The port output data is saved in port latch data register Px. The port modes are configured in port mode control registers PxM0 and PxM1.

When port is configured to analog functions pin by the port alternative control register PxASW, the digital input is disabled.

Some pins are shared with alternative functions, the outside pin function has the highest priority, and the inner pin function has the lowest priority. It means that if the higher priority function is enabled, the lower priority function can't be used even when the lower priority function is also enabled.

15.2 Port Configuration

All port pins on the device may be configured in one of five modes: input only, input with pull-up, input with pull-up, push-pull output or open-drain output.

Each port pin also has a Schmitt-triggered input for improved input noise rejection. During SLEEP mode all the Schmitt-triggered inputs are disabled with the exception of INT0B, INT1B, RSTB, XIN and XOUT. The keyboard alternative pins configured as a keyboard interrupt input will also remain active during STOP mode to wake-up the device. These interrupt pins should either be disabled before entering STOP mode or they should not be left floating.

Table 15-1 Configuration Modes

PxM0.y	PxM1.y	PxRSW	Px.y	Port Mode
0	0	x	x	Input Only (High Impedance)
0	1	0	x	Input with Pull-up
0	1	1	0	Input with Pull-down
0	1	1	1	Input with Pull-up
1	0	x	x	Push-pull Output
1	1	x	x	Open-Drain Output

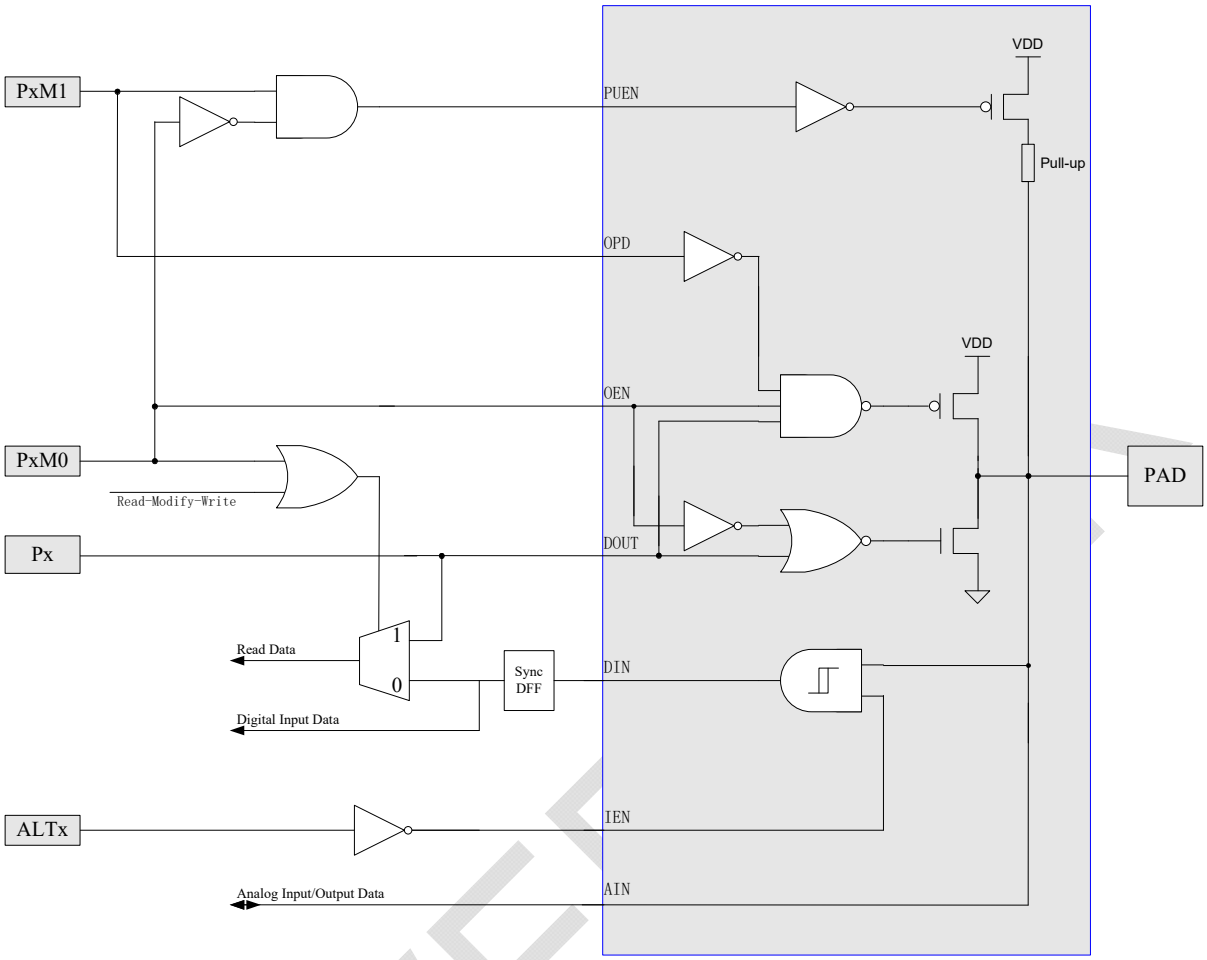


Figure 15-1 GPIO

15.3 Port Analog Functions

The device incorporates an analog comparator and 16-channel touch keys and ADC. In order to give the best analog performance and minimize power consumption, pins that are being used for analog functions must have both their digital outputs and digital inputs disabled.

Digital outputs are disabled by putting the port pins into the input-only mode. Digital inputs are disabled by PxASW(ALTx) whenever analog function pins are enabled and that pin is configured for input-only mode.

15.4 Port Read-Modify-Write

A read from a port will read either the state of the pins or the state of the port register depending on which instruction is used. Simple read instructions will always access the port pins directly.

Read-modify-write instructions, which read a value, possibly modify it, and then write it back, will

always access the port register. This includes bit write instructions such as CLR or SETB as they actually read the entire port, modify a single bit, then write the data back to the entire port.

15.5 Port Alternate Functions

Most general-purpose digital I/O pins of the device share functionality with the various I/Os needed for the peripheral units. The control of port alternate function as below:

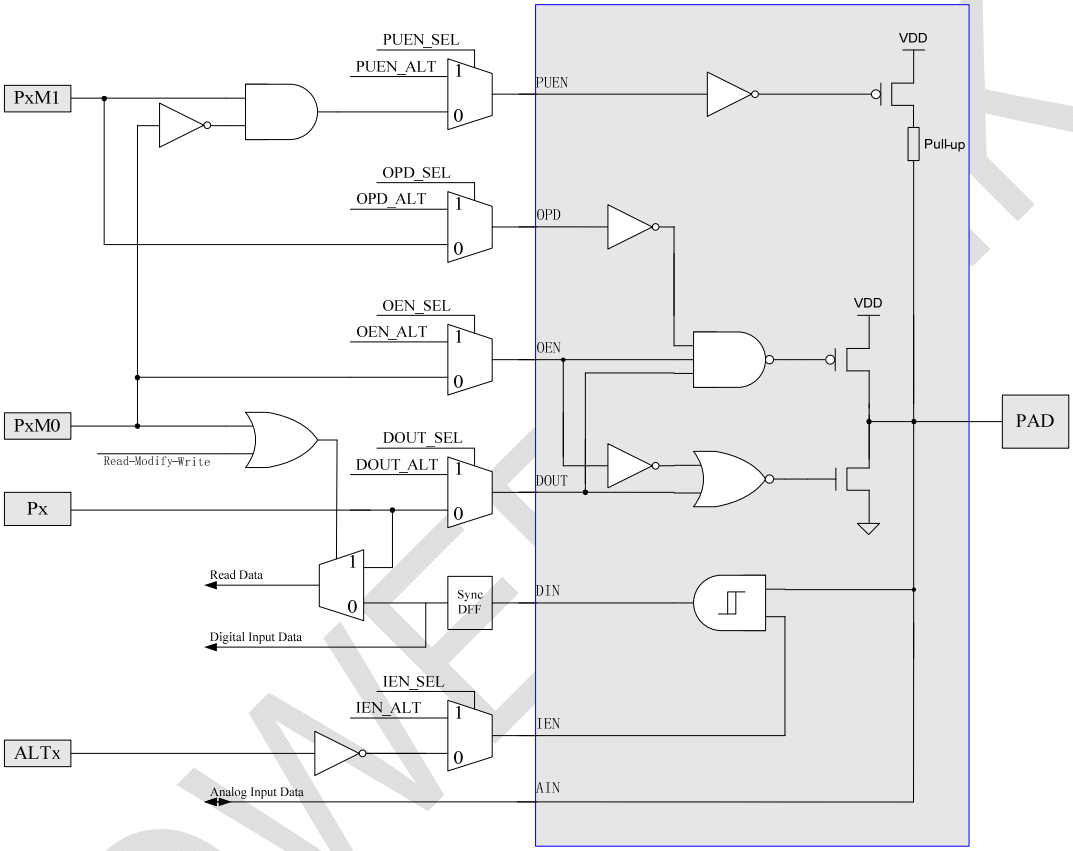


Figure 15-2 Port Alternate Function

Table 15-2 Port Pin Alternate Functions

Symbol	Function	Symbol	Function
RPUEN_SEL	Pull-up Enable Alternate Select	RPUEN_ALT	Pull-up Enable Alternate Control
RPDEN_SEL	Pull-down Enable Alternate Select	RPDEN_ALT	Pull-down Enable Alternate Control
OPD_SEL	Open-Drain Output Enable Alternate Select	OPD_ALT	Open-Drain Output Enable Alternate Control

Symbol	Function		Symbol	Function
OEN_SEL	Output Enable Alternate Select		OEN_ALT	Output Enable Alternate Control
DOUT_SEL	Port Data Output Alternate Select		DOUT_ALT	Port Data Output Alternate Control
IEN_SEL	Digital Input Enable Alternate Select		IEN_ALT	Digital Input Enable Alternate Control
DIN	Digital Input		AIN	Analog Input

15.6 Register Definition

15.6.1 Port 0 Data Register – P0

Table 15-3 P0 Data Register (80h)

Bit	Symbol	Description	Type	Reset
p0.7~6	-	-	R	2'b0
p0.5~0	-	Data register	R/W	6'b0

15.6.2 Port 0 Control Registers – P0M0/P0M1

Table 15-4 P0 Control Register 0 – P0M0 (A1h)

Bit	Symbol	Description	Type	Reset
p0m0.7~6	-	-	R	2'b0
p0m0.5~0	-	Control register 0	R/W	6'b0

Table 15-5 P0 Control Register 1 – P0M1 (A2h)

Bit	Symbol	Description	Type	Reset
p0m1.7~6	-	-	R	2'b0
p0m1.5~0	-	Control register 1	R/W	6'b0

15.6.3 Port 1 Data Register – P1

Table 15-6 P1 Data Register (90h)

Bit	Symbol	Description	Type	Reset
p1.7~0	-	Data register	R/W	00h

15.6.4 Port 1 Control Registers – P1M0/P1M1

Table 15-7 P1 Control Register 0 – P1M0 (A3h)

Bit	Symbol	Description	Type	Reset
p1m0.7~0	-	Control register 0	R/W	00h

Table 15-8 P1 Control Register 1 – P1M1 (A4h)

Bit	Symbol	Description	Type	Reset
p1m1.7~0	-	Control register 1	R/W	00h

15.6.5 Port 2 Data Register – P2

Table 15-9 P2 Data Register (A0h)

Bit	Symbol	Description	Type	Reset
p2.7~0	-	Data register	R/W	00h

15.6.6 Port 2 Control Registers – P2M0/P2M1

Table 15-10 P2 Control Register 0 – P2M0 (A5h)

Bit	Symbol	Description	Type	Reset
p2m0.7~0	-	Control register 0	R/W	00h

Table 15-11 P2 Control Register 1 – P2M1 (A6h)

Bit	Symbol	Description	Type	Reset
p2m1.7~0	-	Control register 1	R/W	00h

15.6.7 PORT Pull Up and Down the Resistance and Analog Port Switch Register – PRASW

Table 15-12 PORT Pull Up nad Down the Resistance and Analog Port Switch Register – PRASW(ABh)

Bit	Symbol	Description	Type	Reset
PRASW.7	-	-	R	0
PRASW.6	p2rsw	PORT2 input pull up and down resistance select	R/W	0
PRASW.5	p1rsw	PORT1 input pull up and down resistance select	R/W	0
PRASW.4	p0rsw	PORT0 input pull up and down resistance select	R/W	0
P0ASW.3~0	-	Port0 analog switch register, control P0.3~0	R/W	0

Note1(pull up and down resistance 100K select): If PxM0 and PxM1 are configured as input without pull up and down resistance, ignore PxRSW; If PxM0 and PxM1 are configured as input with pull up and down resistance, PxRSW=0 select pull-up, PxRSW=1 according to the value of Px.y output register select pull up or pull down(1: pull-up 0: pull-down)

15.6.8 Port Analog Switch Registers – P1ASW/P2ASW

The digital input enable of port1/port2 could be closed or opened accroding to configuration bit of P1ASW/P2ASW, one bit of asw corresponding to one pad, for example, set P1ASW.7 will close port1.7 digital input.

Table 15-13 Port Analog Switch Register 0 – P1ASW (ACh)

Bit	Symbol	Description	Type	Reset
P1ASW.7~0	-	Port1 analog switch register, control port1.7~0	R/W	00h

Table 15-14 Port Analog Switch Register 1 – P2ASW (ADh)

Bit	Symbol	Description	Type	Reset
P2ASW.7~0	-	Port2 analog switch register, control port2.7~0	R/W	00h

15.6.9 Port shift Register – PSFT0

Table 15-15 Port Shift 0 Register (AEh)

Bit	Symbol	Description	Type	Reset
psft0.7	SPI	SCSB/SCK/MISO/MOSI shift control bit	R/W	1'b0

Bit	Symbol	Description	Type	Reset
psft0.6	I2C	SCL/SDA shift control bit	R/W	1'b0
psft0.5	UART0	RXD/TXD shift control bit	R/W	1'b0
psft0.4	INT1B	INT1B shift control bit	R/W	1'b0
psft0.3	INT0B	INT0B shift control bit	R/W	1'b0
psft0.2	T2	T2EX/T2CPO shift control bit	R/W	1'b0
psft0.1	T1	Timer 1 input shift control bit	R/W	1'b0
psft0.0	T0	Timer 0 input shift control bit	R/W	1'b0

15.6.10 Port shift Register – PSFT1

Table 15-16 Port Shift 1 Register (AFh)

Bit	Symbol	Description	Type	Reset
psft 1.7	-	Reserved, keep in 0	R/W	1'b0
psft1.6	DBW	DBW shift control bit	R/W	1'b0
psft1.5	UART1	UART1 shift control bit	R/W	1'b0
psft1.4	BEEPER	BEEPER shift control bit	R/W	1'b0
psft1.3	KEYB	Keyboard 7~0 shift control bit	R/W	1'b0
psft1.2	-	Reserved, keep in 0	R/W	1'b0
psft1.1	PWM1	PWM1 shift control bit	R/W	1'b0
psft1.0	PWM0	PWM0 shift control bit	R/W	1'b0

16 Timer 0 and Timer 1

16.1 Overview

The device has two 16-bit Timer/Counters, Timer 0 and Timer 1.

In the timer mode, the Timer 0/1 is incremented at each active positive edge of clock which is pre-scale of system clock, the pre-scale bits store in the TCON register.

In the counter mode, the Timer 0/1 is incremented when the falling edge is detected at the corresponding input pin – "t0" for Timer 0, "t1" for Timer 1. Since it takes 2 clock cycles to recognize a 1-to-0 event, the maximum input count rate is 1/2 of the oscillator frequency. There are no restrictions on the duty cycle, however to ensure proper recognition of 0 or 1 state, an input should be stable for at least 1 clock cycle.

Four operating modes can be selected for Timer 0/1. Two Special Function Registers: tmod and tcon are used to select the appropriate mode.

16.2 Mode 0 and Mode 1

In mode 0, Timer 0 is configured as a 13-bit register ("tl0" = 5 bits, "th0" = 8 bits). The upper 3 bits of "tl0" are unchanged and should be ignored.

In mode 1, Timer 0 is configured as a 16- bit register.

In mode 0, Timer 1 is configured as a 13-bit register ("tl1" = 5 bits, "th1" = 8 bits). The upper 3 bits of "tl1" are unchanged and should be ignored.

In mode 1, Timer 1 is configured as a 16- bit register.

Timer 1 in Mode 0 or Mode 1 are the same as Timer 0, all have 13-bit prescaler.

The timer clock source is controlled by TCKCON.TPSx.

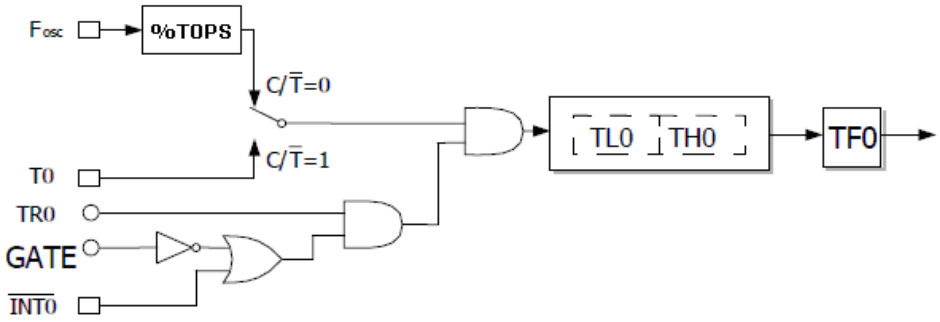


Figure 16-1 Timer 0 in Mode 0 and 1

16.3 Mode 2

In this mode the Timer 0 and Timer 1 are configured as an 8-bit register with auto-reload.

Timer 1 in Mode 2 are the same as Timer 0.

The timer clock source is controlled by TCKCON.TPSx.

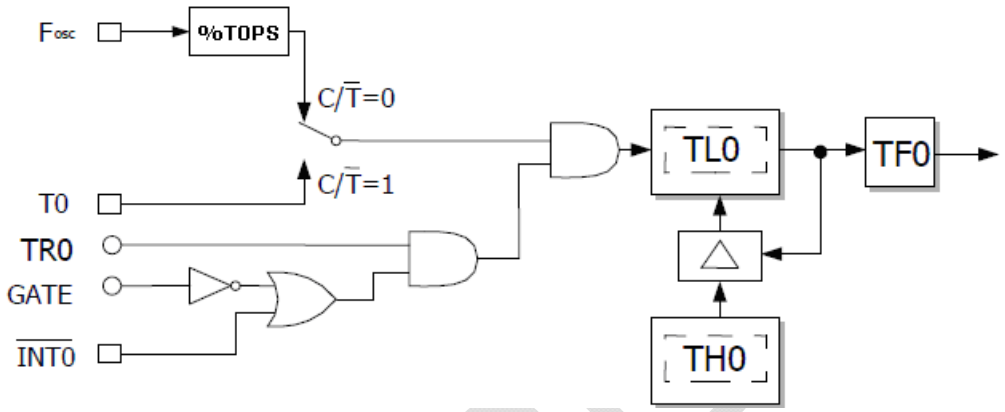


Figure 16-2 Timer 0 in Mode 2

16.4 Mode 3

In mode 3, Timer 0 is configured as one 8-bit timer/counter and one 8-bit timer.

When Timer 0 works in mode 3, Timer 1 can still be used in other mode by the serial port as a baud rate generator, or application not requiring an interrupt from Timer 1.

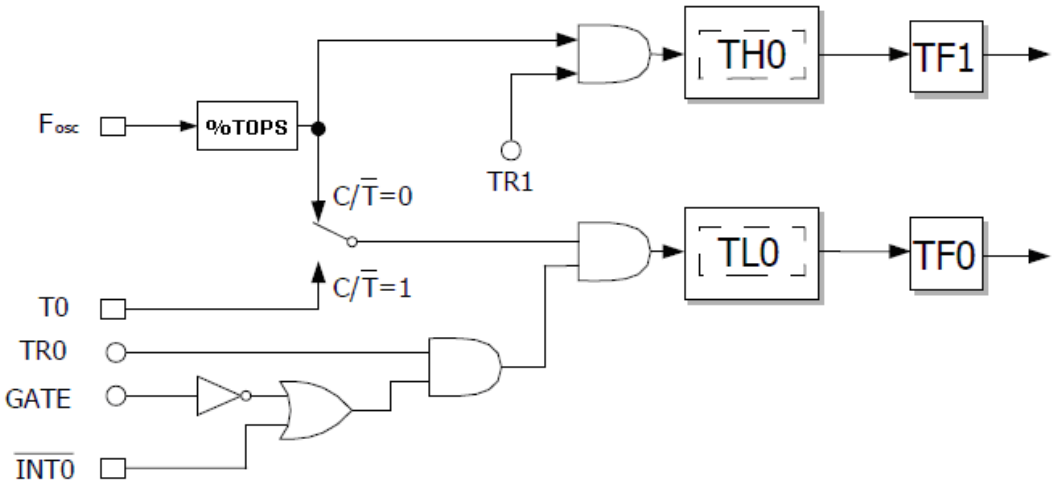


Figure 16-3 Timer 0 in Mode 3

16.5 Register Definition

16.5.1 Timer/Counter Control Register - TCON

Table 16-1 TCON Register (88h)

Bit	Symbol	Description	Type	Reset
tcon.7	tf1	**Timer 1 overflow flag** Bit set by hardware when Timer1 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.	R/W	0
tcon.6	tr1	**Timer1 Run control** If cleared, Timer 1 stops.	R/W	0
tcon.5	tf0	**Timer 0 overflow flag** Bit set by hardware when Timer 0 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.	R/W	0
tcon.4	tr0	**Timer 0 Run control** If cleared, Timer 0 stops.	R/W	0
tcon.3	if1	**External interrupt 1 flag** Set by hardware, when external interrupt int1 (edge/level, depending on settings) is observed. Cleared by hardware when interrupt is processed.	R/W	0*
tcon.2	it1	**External interrupt 1 type control** **<it1_inv = 0>** 1: activated at falling edge 0: activated at low level **<it1_inv = 1>** 1: activated at rising edge 0: activated at high level	R/W	0
tcon.1	if0	**External interrupt 0 flag** Set by hardware, when external interrupt int0 (edge/level, depending on settings) is observed. Cleared by hardware when interrupt is processed.	R/W	0*
tcon.0	it0	**External interrupt 0 type control** **<it1_inv = 0>** 1: activated at falling edge 0: activated at low level **<it1_inv = 1>** 1: activated at rising edge 0: activated at high level	R/W	0

Note: After power on, the register perhaps read out as '0Ah' when the INT0B/INT1B port is input floating, that means there are interrupt flags for INT0B/INT1B, if happenning, clear these flags before using the INT0B/INT1B interrupt is strongly recomendded.

16.5.2 Timer Mode Register - TMOD

Table 16-2 TMOD Register (89h)

Bit	Symbol	Description	Type	Reset
tmod.7	Gate	**Timer 1 gate control** If set, enables external gate control (pin "int(1)") for Counter 1. When "int(1)" is high, and "tr1" bit is set (Table 18), the Counter 1 is incremented every falling edge on "t1" input pin	R/W	0
tmod.6	c/t	**Timer 1 counter/timer select** Selects Timer or Counter operation. When set to 1, a Counter operation is performed, when cleared to 0, the Timer/Counter 1 will function as a Timer.	R/W	0
tmod.5	m1	**Timer 1 mode** Selects mode for Timer/Counter 1, as shown in table below.	R/W	0
tmod.4	m0		R/W	0
tmod.3	Gate	**Timer 0 gate control** If set, enables external gate control (pin "int(0)") for Counter 0. When "int(0)" is high, and "tr0" bit is set (Table 18), the Counter 0 is incremented every falling edge on "t0" input pin	R/W	0
tmod.2	c/t	**Timer 0 counter/timer select** Selects Timer or Counter operation. When set to 1, a Counter operation is performed, when cleared to 0, the Timer/Counter 0 will function as a Timer.	R/W	0
tmod.1	m1	**Timer 0 mode** Selects mode for Timer/Counter 0, as shown in table below.	R/W	0
tmod.0	m0		R/W	0

Table 16-3 Timers/Counters Modes

M1	M0	Mode	Function
0	0	Mode 0	13-bit Counter/Timer, with 5 lower bits in tl0 (tl1) register and 8 bits in th0 (th1) register (for Timer 0 or Timer 1, respectively). Note, that unlike in 80C51, the 3 high-order bits of tl0 (tl1) are zeroed whenever Mode 0 is enabled.
0	1	Mode 1	16-bit Counter/Timer.
1	0	Mode 2	8-bit auto-reload Counter/Timer. The reload value is kept in th0 (th1), while tl0 (tl1) is incremented every machine cycle. When tl0 (tl1) overflows, a value from th0 (th1) is

M1	M0	Mode	Function
			copied to tl0 (tl1).
1	1	Mode 3	For Timer1: Timer1 is stopped. For Timer0: Timer 0 acts as two independent 8 bit Timers/Counters – tl0, th0. - tl0 uses the Timer0 control bits and sets tf0 flag on overflow - th0 operates as timer1. It is enabled by tr1 bit and sets tf1 flag on overflow.

16.5.3 Timer Clock Prescaler Register - TCKCON

Table 16-4 TCKCON Register (8Fh)

Bit	Symbol	Description	Type	Reset
tckcon.7	-	-	R	0
tckcon.6	t2ps2	**Timer 2 Prescaler selection**	R/W	1
tckcon.5	t2ps1		R/W	0
tckcon.4	t2ps0		R/W	0
tckcon.3	t1ps1	**Timer 1 Prescaler selection**	R/W	1
tckcon.2	t1ps0		R/W	1
tckcon.1	t0ps1	**Timer 0 Prescaler selection**	R/W	1
tckcon.0	t0ps0		R/W	1

Table 16-5 Timer 2 Clock Prescaler Selection

T2PS2	T2PS1	T2PS0	Timer 2 Clock Prescaler Selection
0	0	0	RSV
0	0	1	clk_sys/2
0	1	0	clk_sys/4
0	1	1	clk_sys/8
1	0	0	clk_sys/12
1	0	1	clk_sys/16
1	1	0	clk_sys/32
1	1	1	clk_sys/128

Table 16-6 Timer 1/0 Clock Prescaler Selection

T1PS1	T1PS0	Timer 1 Clock Prescaler		T0PS1	T0PS0	Timer 0 Clock Prescaler
0	0	RSV		0	0	RSV
0	1	clk_sys/4		0	1	clk_sys/4
1	0	clk_sys/8		1	0	clk_sys/8

T1PS1	T1PS0	Timer 1 Clock Prescaler		T0PS1	T0PS0	Timer 0 Clock Prescaler
1	1	clk_sys/12		1	1	clk_sys/12

16.5.4 Timer 0 Registers – TH0/TL0

Table 16-7 TH0 Register (8Ch)

Bit	Symbol	Description	Type	Reset
th0.7~0	-	Timer 0 higher byte	R/W	00h

Table 16-8 TL0 Register (8Ah)

Bit	Symbol	Description	Type	Reset
tl0.7~0	-	Timer 0 lower byte	R/W	00h

16.5.5 Timer 1 Registers – TH1/TL1

Table 16-9 TH1 Register (8Dh)

Bit	Symbol	Description	Type	Reset
th1.7~0	-	Timer 1 higher byte	R/W	00h

Table 16-10 TL1 Register (8Bh)

Bit	Symbol	Description	Type	Reset
tl1.7~0	-	Timer 1 lower byte	R/W	00h

17 Timer 2

17.1 Overview

The device includes a 16-bits Timer with Compare/Capture and PWM.

17.2 Timer Function

The Timer 2 can operate as 16-bits timer.

17.2.1 Timer Mode

In this mode, the count rate is derived from the prescaler of system clock. The prescaler mode is controlled by TCKCON.T2PS. Set T2CON.T2EN to start timer counting.

17.2.2 Timer 2 Reload Mode

A 16-bits reload from the Timer2 Compare/Capture registers can be executed in two reload modes:

- Mode 0: Reload signal is generated by Timer 2 overflow (auto reload)
- Mode 1: Reload signal is generated by negative transition at the corresponding input pin T2EX.

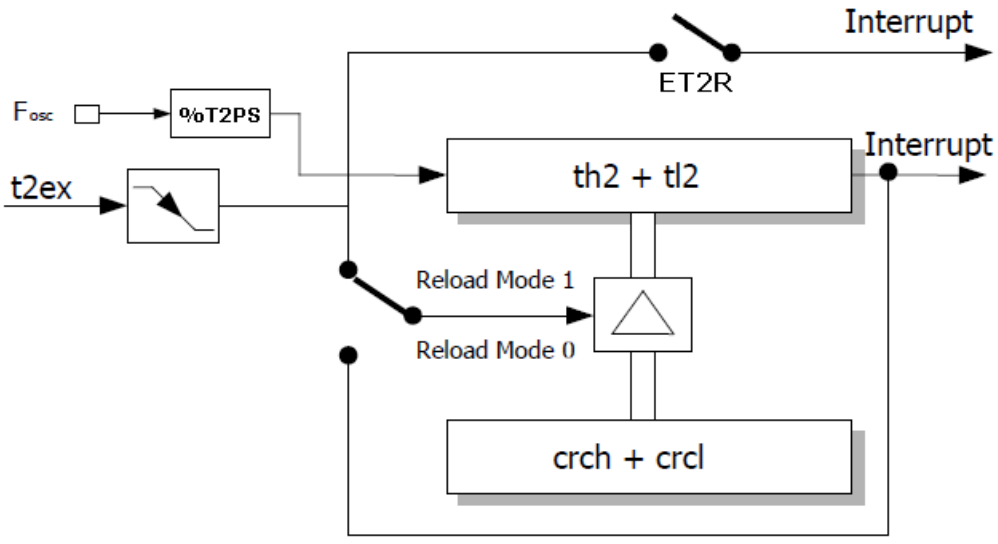


Figure 17-1 Timer 2 in Reload Mode

17.3 Compare Function

The Compare/Capture consists of one 16-bits Timer 2 compare data register. The register can be configured to work in comparator mode. In this mode the value stored in register is compared with the contents of the Timer2. The comparators outputs drive the T2CPO pin, where the T2CPO is output of the comparator associated with the register CRCH/CRCL.

There are two compare modes selected by T2CON.T2CM.

17.3.1 Compare Mode 0

In mode 0, when the value in Timer 2 equals the value of the compare register, the comparator output changes from low to high. It goes back low on timer 2 overflow.

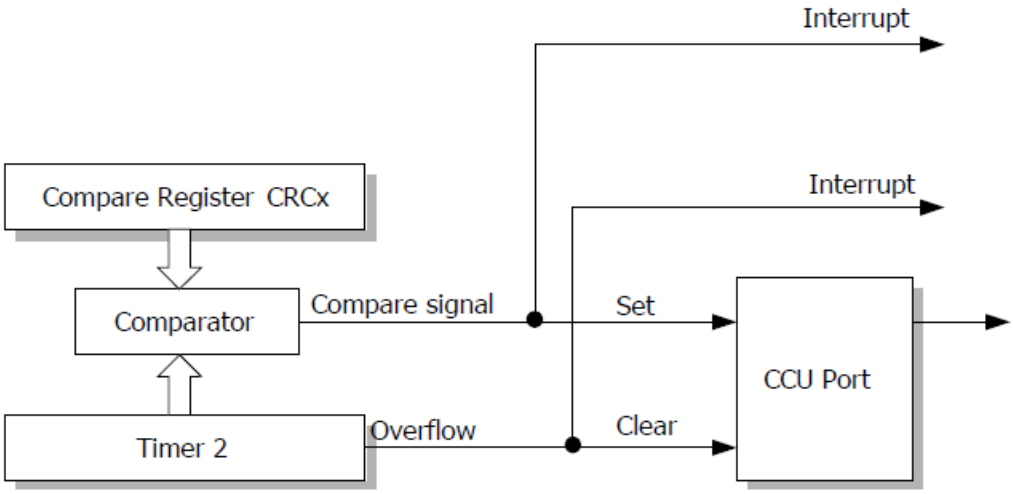


Figure 17-2 Timer 2 in Compare Mode 0

17.3.2 Compare Mode 1

In compare mode 1, the transition of the output signal can be determined by software. A Timer 2 overflow causes no output change. In this mode both transitions of output signal can be controlled. Figure below shows a functional diagram of a register/port configuration in compare mode 1. In compare mode 1 the value is written first to the “Shadow Register (p0.3/p1.7)”, and when the compare signal goes active this value is transferred to the output register.

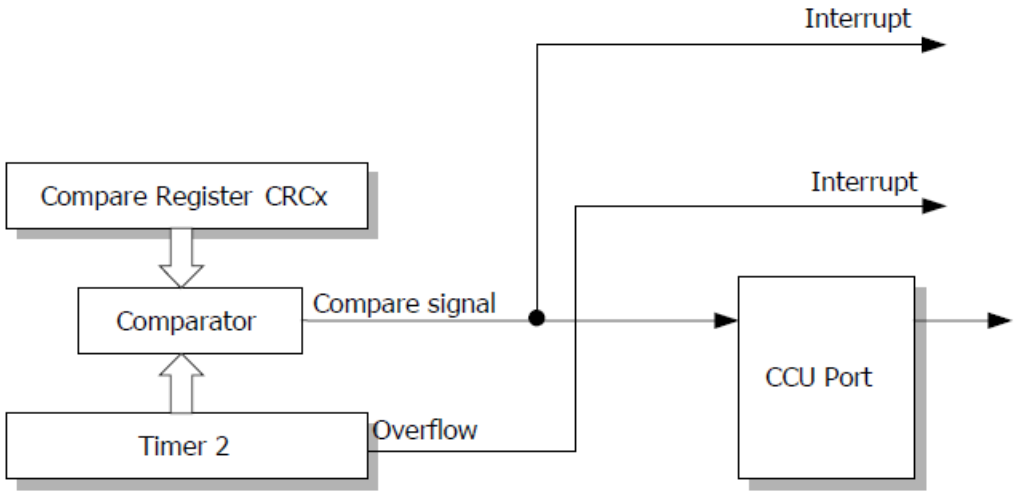


Figure 17-3 Timer 2 in Compare Mode 1

17.4 Capture Function

The 16-bits CRCH/CRCL register can be configured to work in capture mode.

In this mode the actual timer/counter contents are saved into the CRCH/CRCL register upon an internal event (mode 0) or a software write operation (mode 1).

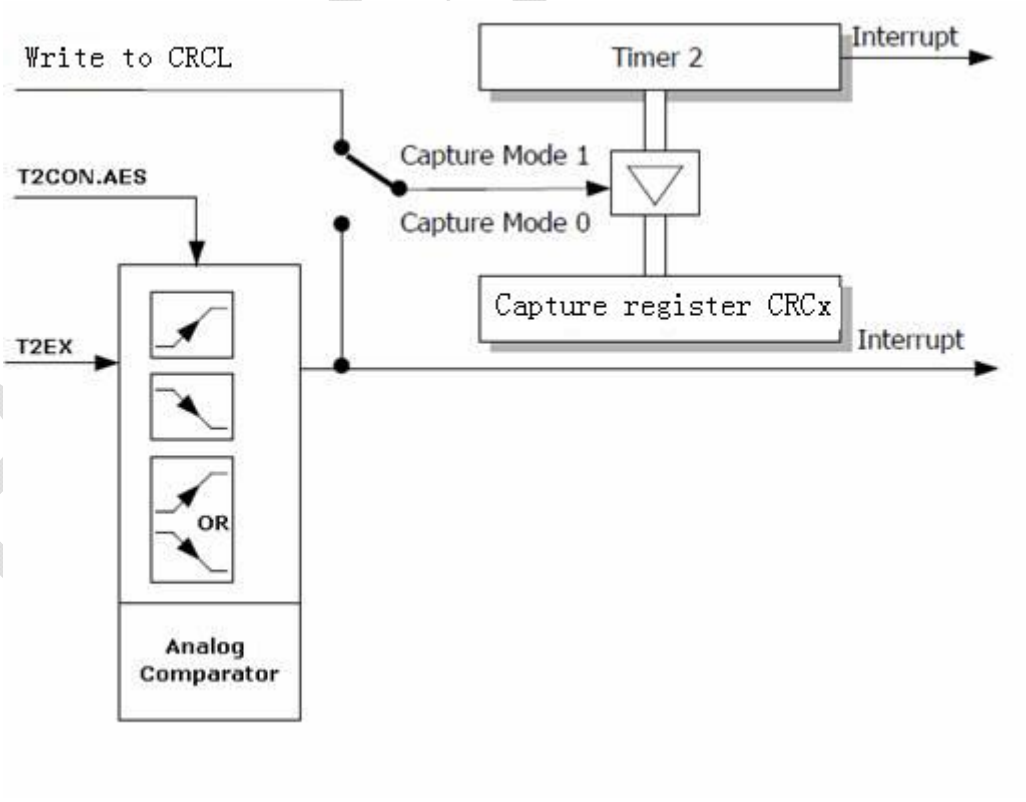


Figure 17-4 Timer 2 in Capture Mode

17.4.1 Capture Mode 0

In mode 0 capturing of Timer 2 contents is executed when rising edge, falling edge, toggle edge on T2EX or analog comparator output trigger depending on the T2CON.AES.
The timer 2 contents will be latched into appropriate capture register CRCH/CRCL. In this mode no interrupt request will be generated.

17.4.2 Capture Mode 1

In mode 1 capture of Timer 2 is caused by any write into the low-ordered byte of the dedicated capture register. The value written to capture register is irrelevant for this function. The Timer 2 contents will be latched into appropriate capture register CRCH/CRCL. In this mode no interrupt request will be generated.

17.5 PWM Function

The 16-bits CRCH/CRCL registers can be configured for 8-bit PWM mode.

In PWM mode, TL2 will be used as PWM period register, CRCL will be used as PWM duty register, and TH2 will be used as PWM counter.

Note: PWM duty is calculated using duty register CRCL/period register TL2.

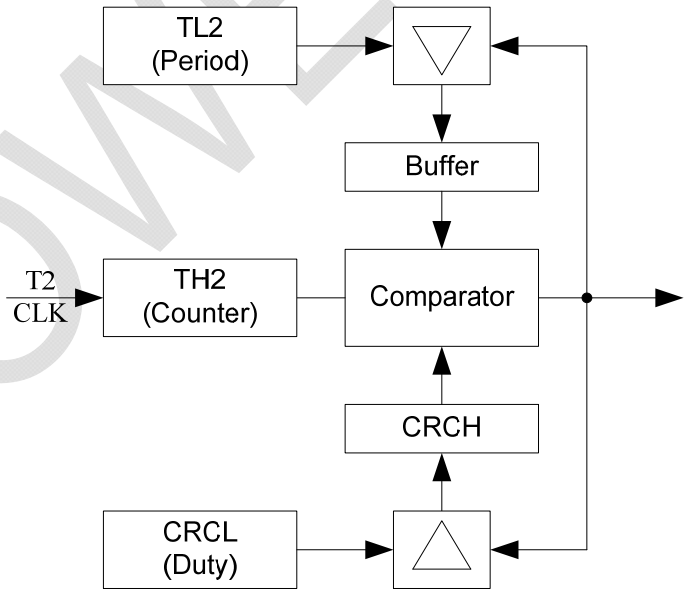


Figure 17-5 Timer 2 in PWM Mode

17.6 Register Definition

17.6.1 Timer 2 Control Register – T2CON

Table 17-1 T2CON Register (C8h)

Bit	Symbol	Description	Type	Reset
t2con.7	t2en	**Timer 2 enable** 0 – Timer/Compare/Capture/PWM mode disabled 1 – Timer/Compare/Capture/PWM mode enabled	R/W	0
t2con.6	aes1	**Active edge selection**	R/W	0
t2con.5	aes0	For Timer 2 Compare/Capture/PWM mode	R/W	0
t2con.4	t2r1	**Timer 2 reload mode selection**	R/W	0
t2con.3	t2r0	0x – reload disabled 10 – Mode 0 11 – Mode 1	R/W	0
t2con.2	t2cm	**Timer 2 compare mode selection** 0 – Mode 0 1 – Mode 1	R/W	0
t2con.1	it1_inv	**External interrupt 1 triggers mode set to reverse** **<it1_sel = 2'b00>/<it1_sel != 2'b00>** **indicates the FILTER enablement position of INT1** 0：INT1B does not filter burrs 1：INT1B filter 5ns burr	R/TW	0
t2con.0	it0_inv	**External interrupt 0 triggers mode set to reverse** **<it1_sel = 2'b00>/<it1_sel != 2'b00>** **indicates the FILTER enablement position of INT0** 0：INT1B does not filter burrs 1：INT1Bfilter 5ns burr	R/TW	0

Table 17-2 T2 Active Edge Selection

AES1	AES0	Compare Mode	Capture Mode	PWM Mode
0	0	-	Falling Edge	CCP overflow output low Timer 2 Overflow output high
0	1	-	Rising Edge	CCP overflow output high Timer 2 Overflow output low
1	0	-	Toggle Edge	-
1	1	-	Analog Comparator	-

17.6.2 Timer 2 Mode Register – T2MOD

Table 17-3 T2MOD Register (C9h)

Bit	Symbol	Description	Type	Reset
t2mod.7	S0BDS	Serial port 0 baud rate select**(Mode 1/3)** 0: Timer1 Overflow 1: Register S0BDL、S0BDH	R/W	0
t2mod.6	S0BDD	Serial port 0 baud rate doubled select (1: baud rate doubled)	R/W	0
t2mod.5	LSMSR	Low speed 32KHz measure enable 0: Disable 1: Enable measure CLK32K through T2EX input	R/TW	0
t2mod.4~3			R	00b
t2mod.2	-	**Timer 2 Compare/Capture mode selection**	R/W	0
t2mod.1	-		R/W	0
t2mod.0	-		R/W	0

Table 17-4 Timer 2 Compare/Capture Mode Selection

T2MOD.2	T2MOD.1	T2MOD.0	Timer 2 Mode
0	0	0	Timer mode
0	0	1	Capture mode 0
0	1	0	Capture mode 1
0	1	1	Compare mode, disable output
1	0	0	Compare mode, enable output to T2CPO
1	0	1	PWM output to T2CPO
1	1	0	Timer mode
1	1	1	Timer mode

17.6.3 Timer 2 Compare/Reload/Capture/PWM Registers – CRCH/CRCL

Table 17-5 CRCH Register (CBh)

Bit	Symbol	Description	Type	Reset
crch.7~0	-	Timer 2 Compare/Reload/Capture/PWM Register	R/W	00h

Table 17-6 CRCL Register (CAh)

Bit	Symbol	Description	Type	Reset
crcl.7~0	-	Timer 2 Compare/Reload/Capture/PWM Register	R/W	00h

17.6.4 Timer 2 Registers – TH2/TL2

Table 17-7 TH2 Register (CDh)

Bit	Symbol	Description	Type	Reset
th2.7~0	-	Timer 2 higher byte	R/W	00h

Table 17-8 TL2 Register (CCh)

Bit	Symbol	Description	Type	Reset
tl2.7~0	-	Timer 2 lower byte	R/W	00h

18 PWM0/1/2/3/4/5

18.1 Overview

The device includes six 12-bit pulse width modulation (PWM) output. The SFR PWMEN and PWMxCON are PWM mode control register, the SFRs PWMxDH/PWMxDL are PWM duty cycle control registers, and the SFRs PWMxPH/PWMxPL are PWM period cycle control registers. PWM0/3 share PWM0 period cycle register and control bit, PWM1/4 share PWM1 period cycle register and control bit, PWM2/5 share PWM2 period cycle register and control bit.

Each PWM part has four working mode:

- Standard
- Set high level when matched
- Toggles when matched
- Center-aligned

In PWM mode, when set the duty cycle control registers or set the period cycle control registers, the high byte register should be set firstly, and then set the low byte register. Once the low byte register is set, the data will be loaded and PWM will start working.

Note: PWM duty is calculated using duty register PWMxD+1/period register PWMxP+1.

PWM can work in IDLE mode, and be disabled in STOP mode.

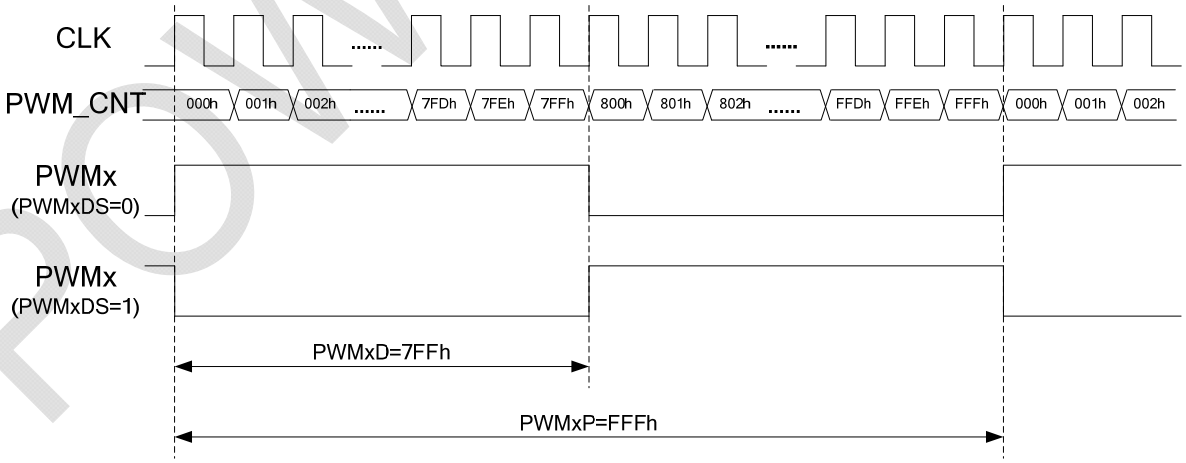


Figure 18-1 12-bit PWM standard mode

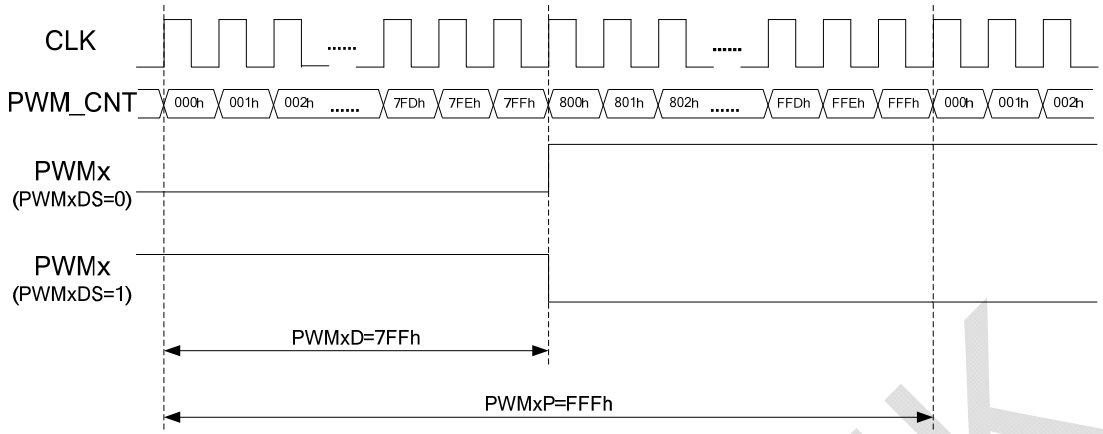


Figure 18-2 PWM matched set high level mode

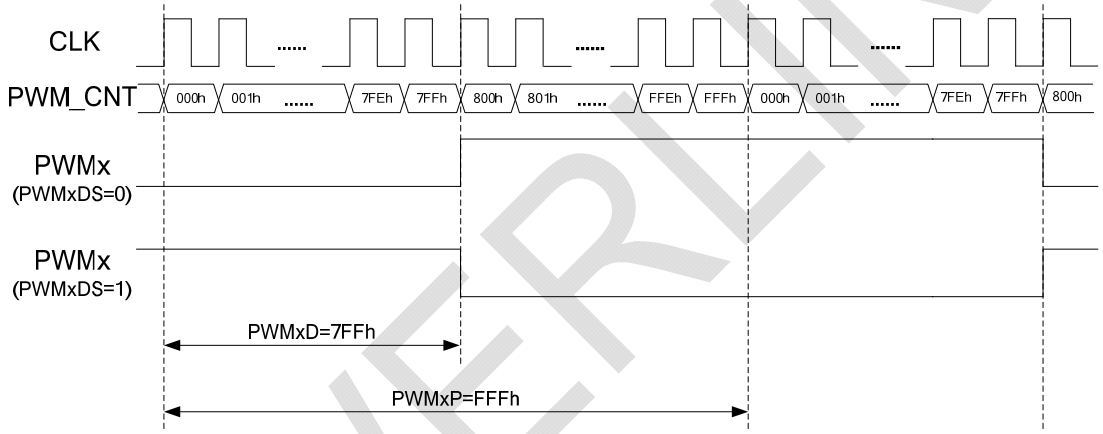


Figure 18-3 PWM matched toggle mode

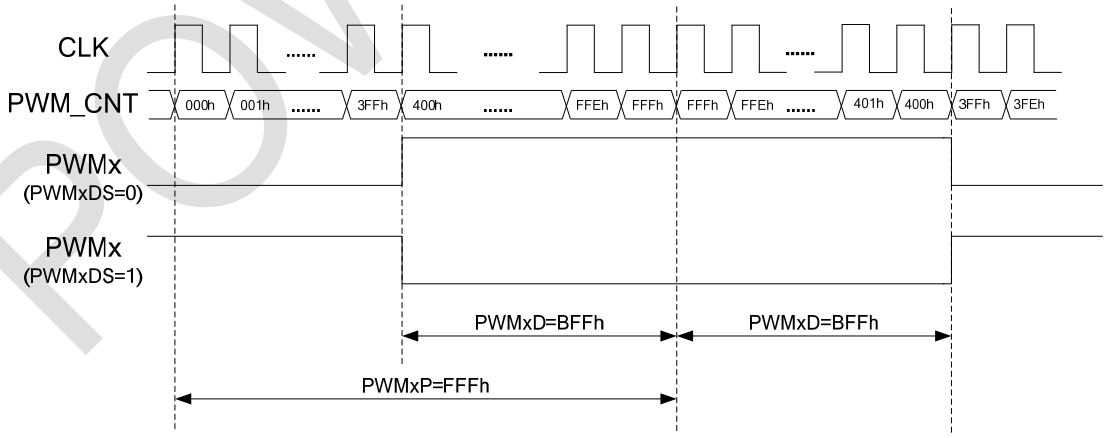


Figure 18-4 PWM Center-aligned mode

18.2 Register Definition

18.2.1 PWM Control Register – PWMEN

Table 18-1 PWMEN Register (F9h)

Bit	Sympol	Descriprion	Type	Reset
pwmen.7	-	-	R	0
pwmen.6	-	-	R	0
pwmen.5	pwm5en	**PWM5 enable**	R/W	0
pwmen.4	pwm4en	**PWM4 enable**	R/W	0
pwmen.3	pwm3en	**PWM3 enable**	R/W	0
pwmen.2	pwm2en	**PWM2 enable**	R/W	0
pwmen.1	pwm1en	**PWM1 enable**	R/W	0
pwmen.0	pwm0en	**PWM0 enable**	R/W	0

18.2.2 PWM Control Register – PWM0CON

Table 18-2 PWM0CON Register (FAh)

Bit	Symbol	Description	Type	Reset
pwm0con.7	pwm0ds	**PWM0 duty polarity selection** 0: Normal duty polarity mode, output active high level 1: Negative duty polarity mode, output active low level	R/W	0
pwm0con.6	pwm0ms1	**PWM0 working mode selection**	R/W	0
pwm0con.5	pwm0ms0	00 – Standard 01 – Set high level when matched 10 – Toggles when matched 11 – Center-aligned	R/W	0
pwm0con.4	pwm0cs1	**PWM0 clock source selection**	R/W	0
pwm0con.3	pwm0cs0		R/W	0
pwm0con.2	pwm0ps2	**PWM0 clock prescaler selection**	R/W	0
pwm0con.1	pwm0ps1		R/W	0
pwm0con.0	pwm0ps0		R/W	0

18.2.3 PWM Control Register – PWM1CON

Table 18-3 PWM1CON Register (F2h)

Bit	Symbol	Description	Type	Reset
pwm1con.7	pwm1ds	**PWM1 duty polarity selection** 0: Normal duty polarity mode, output active high level 1: Negative duty polarity mode, output active low level	R/W	0
pwm1con.6	pwm1ms1	**PWM1 working mode selection**	R/W	0
pwm1con.5	pwm1ms0	00 – Standard 01 – Set high level when matched 10 – Toggles when matched 11 – Center-aligned	R/W	0
pwm1con.4	pwm1cs1	**PWM1 clock source selection**	R/W	0
pwm1con.3	pwm1cs0		R/W	0
pwm1con.2	pwm1ps2	**PWM1 clock prescaler selection**	R/W	0
pwm1con.1	pwm1ps1		R/W	0
pwm1con.0	pwm1ps0		R/W	0

18.2.4 PWM Control Register – PWM2CON

Table 18-4 PWM2CON Register (EAh)

Bit	Symbol	Description	Type	Reset
pwm2con.7	pwm2ds	**PWM2 duty polarity selection** 0: Normal duty polarity mode, output active high level 1: Negative duty polarity mode, output active low level	R/W	0
pwm2con.6	pwm2ms1	**PWM2 working mode selection**	R/W	0
pwm2con.5	pwm2ms0	00 – Standard 01 – Set high level when matched 10 – Toggles when matched 11 – Center-aligned	R/W	0
pwm2con.4	pwm2cs1	**PWM2 clock source selection**	R/W	0
pwm2con.3	pwm2cs0		R/W	0
pwm2con.2	pwm2ps2	**PWM2 clock prescaler selection**	R/W	0
pwm2con.1	pwm2ps1		R/W	0
pwm2con.0	pwm2ps0		R/W	0

Table 18-5 PWM Prescaler Selection

PWMxCS1	PWMxCS0	PWMx Clock Selection
0	0	clk_per

PWMxCS1	PWMxCS0	PWMx Clock Selection
0	1	clk_hirc (Keep work in STOP mode, inactive in SLEEP mode)
1	0	clk_lirc (Keep work in STOP&SLEEP mode)
1	1	Reserved, just used for internal test

Table 18-6 PWM Prescaler Selection

PWMxPS2	PWMxPS1	PWMxPS0	PWMx Clock Prescaler Selection
0	0	0	clk_pwm/1
0	0	1	clk_pwm/2
0	1	0	clk_pwm/4
0	1	1	clk_pwm/8
1	0	0	clk_pwm/16
1	0	1	clk_pwm/32
1	1	0	clk_pwm/64
1	1	1	clk_pwm/128

18.2.5 PWM0 Period Registers – PWM0PH/PWM0PL

Table 18-7 PWM0PH Register (FCh)

Bit	Symbol	Description	Type	Reset
pwm0ph.7~4	-	-	R	4'b0
pwm0ph.3~0	-	PWM0 period cycle register higher byte	R/W	4'b0

Table 18-8 PWM0PL Register (FBh)

Bit	Symbol	Description	Type	Reset
pwm0pl.7~0	-	PWM0 period cycle register lower byte	R/W	00h

18.2.6 PWM0 Duty Registers – PWM0DH/PWM0DL

Table 18-9 PWM0DH Register (FEh)

Bit	Symbol	Description	Type	Reset
pwm0dh.7~4	-	-	R	4'b0
pwm0dh.3~0	-	PWM0 duty cycle register higher byte	R/W	4'b0

Table 18-10 PWM0DL Register (FDh)

Bit	Symbol	Description	Type	Reset
pwm0dl.7~0	-	PWM0 duty cycle register lower byte	R/W	00h

18.2.7 PWM1 Period Registers – PWM1PH/PWM1PL

Table 18-11 PWM1PH Register (F4h)

Bit	Symbol	Description	Type	Reset
pwm1ph.7~4	-	-	R	4'b0
pwm1ph.3~0	-	PWM1 period cycle register higher byte	R/W	4'b0

Table 18-12 PWM1PL Register (F3h)

Bit	Symbol	Description	Type	Reset
pwm1pl.7~0	-	PWM1 period cycle register lower byte	R/W	00h

18.2.8 PWM1 Duty Registers – PWM1DH/PWM1DL

Table 18-2 PWM1DH Register (F6h)

Bit	Symbol	Description	Type	Reset
pwm1dh.7~4	-	-	R	4'b0
pwm1dh.3~0	-	PWM1 duty cycle register higher byte	R/W	4'b0

Table 18-3 PWM1DL Register (F5h)

Bit	Symbol	Description	Type	Reset
pwm1dl.7~0	-	PWM1 duty cycle register lower byte	R/W	00h

18.2.9 PWM2 Period Registers – PWM2PH/PWM2PL

Table 18-4 PWM2PH Register (ECh)

Bit	Symbol	Description	Type	Reset
pwm2ph.7~4	-	-	R	4'b0
pwm2ph.3~0	-	PWM2 period cycle register higher byte	R/W	4'b0

Table 18-5 PWM2PL Register (EBh)

Bit	Symbol	Description	Type	Reset
pwm2pl.7~0	-	PWM2 period cycle register lower byte	R/W	00h

18.2.10 PWM2 Duty Registers – PWM2DH/PWM2DL

Table 18-6 PWM2DH Register (EEh)

Bit	Symbol	Description	Type	Reset
pwm2dh.7~4	-	-	R	4'b0
pwm2dh.3~0	-	PWM2 duty cycle register higher byte	R/W	4'b0

Table 18-7 PWM2DL Register (EDh)

Bit	Symbol	Description	Type	Reset
pwm2dl.7~0	-	PWM2 duty cycle register lower byte	R/W	00h

18.2.11 PWM3 Duty Registers – PWM3DH/PWM3DL

Table 18-8 PWM3DH Register E6h)

Bit	Symbol	Description	Type	Reset
pwm3dh.7~4	-	-	R	4'b0
pwm3dh.3~0	-	PWM3 duty cycle register higher byte	R/W	4'b0

Table 18-20 PWM3DL Register (E5h)

Bit	Symbol	Description	Type	Reset
pwm3dl.7~0	-	PWM3 duty cycle register lower byte	R/W	00h

18.2.12 PWM4 Duty Registers – PWM4DH/PWM4DL

Table 18-21 PWM4DH Register (E4h)

Bit	Symbol	Description	Type	Reset
pwm4dh.7~4	-	-	R	4'b0
pwm4dh.3~0	-	PWM4 duty cycle register higher byte	R/W	4'b0

Table 18-22 PWM4DL Register (E3h)

Bit	Symbol	Description	Type	Reset
pwm4dl.7~0	-	PWM4 duty cycle register lower byte	R/W	00h

18.2.13 PWM5 Duty Registers – PWM5DH/PWM5DL

Table 18-23 PWM5DH Register (E2h)

Bit	Symbol	Description	Type	Reset
pwm5dh.7~4	-	-	R	4'b0
pwm5dh.3~0	-	PWM5 duty cycle register higher byte	R/W	4'b0

Table 18-24 PWM5DL Register (E1h)

Bit	Symbol	Description	Type	Reset
pwm5dl.7~0	-	PWM5 duty cycle register lower byte	R/W	00h

19 Watchdog Timer

The device has a watchdog timer (WDT), the watchdog timer is an 18-bit counter. It is used to provide the system supervision in case of software or hardware upset. If the software is not able to refresh the WDT before it is time-out, an internal reset is generated. Software can access (read or write) the RSTCON.WDRF to reset the WDT counter and re-open a WDT window.

19.1 Register Definition

19.1.1 WDT Control Register – WDTCON

Table 19-1 WDTCON Register (86h)

Bit	Symbol	Description	Type	Reset
wdtcon.7	wdten	**WDT enable** 0 – disabled 1 – enabled If WDTEN_INV is 0, power-on default value is 0; If WDTEN_INV is 1, power-on default value is 1;	R/TW	0
wdtcon.6	-	-	R	0
wdtcon.5	wdtien	**WDT interrupt enable** 0 – disable 1 – enable	R/W	0
wdtcon.4	wdtif	**WDT interrupt flag** when enabled, the flag indicating the WDT timeout reset interrupt happen.	R/W	0
wdtcon.3	wdtps3	**WDT prescaler selection**	R/TW	0
wdtcon.2	wdtps2		R/TW	0
wdtcon.1	wdtps1		R/TW	0
wdtcon.0	wdtps0		R/TW	0

Table 19-2 WDT Prescaler Selection

WDTPS3	WDTPS2	WDTPS1	WDTPS0	Time-out Cycles	Time-out (Typ.)
0	0	0	0	512	16ms
0	0	0	1	1024	31ms
0	0	1	0	2048	63ms
0	0	1	1	4096	125ms
0	1	0	0	8192	250ms

WDTPS3	WDTPS2	WDTPS1	WDTPS0	Time-out Cycles	Time-out (Typ.)
0	1	0	1	16384	500ms
0	1	1	0	32768	1.0s
0	1	1	1	65536	2.0s
1	0	0	0	131072	4.0s
1	0	0	1	262144	8.0s
1	0	1	0	Reserved	Reserved
1	0	1	1	Reserved	Reserved
1	1	0	0	64	2.0ms
1	1	0	1	32	1.0ms
1	1	1	0	16	0.5ms
1	1	1	1	8	0.25ms

20 Deadband Waveform Generator DBW0/1/2

20.1 Overview

Deadband waveform generator (DBW) can generate complementary waveforms with deadband delay from selected input source. The DBW has following features:

- Optional deadband clock source control
- Optional input source
- Output enable control
- Output polarity control
- Deadband control by separate 6-bit rising edge and falling edge deadband counter
- Automatic shutdown control by following function:
  - Optional shutdown source
  - Automatic restart enable
  - Automatic shutdown pin rewrite control

20.2 Basic operation

DBW generate two output waveform base on selected input source. The change of each output from off to on may be delayed by the change of other output from off to on result in an immediate delay, during which two output are not driven. This called deadband.

There may need to prevent circuit failure occurred, feedback event arriving late or not arriving at all. In this case, the active drive must be terminated before the failure caused damage, which is called automatic shutdown.

DBW module allow to select following clock source: (select proper clock source in sleep mode)

- ✧ GxIS selected PWM clock (note: PWM clock is configured by PWMxCS)
- ✧ CLKPER

The input source of DBW module can be ACMP1, PWM0~5, DBW input and T2CPO(PWM), which is configured by GxIS.

After enable DBW module, configure complementary driver immediately and clear DBWxA and DBWxB driver. Each DBW output polarity can be configured by GxPOLA and GxPOLB independently select.

20.3 Deadband control

Deadband control is used to provide non-overlapping output signals to prevent through current

generation in power switches. DBW contains two 6-bit deadband counter, one for rising edge and one for falling edge of input source control.

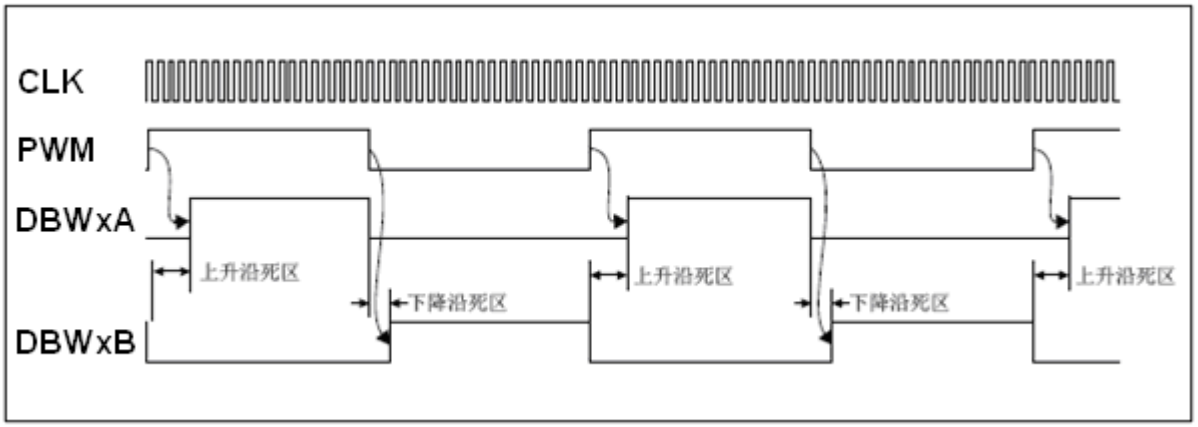


Figure 20-1 Typical DBW waveform

The DBWxA output is delayed when DBWxB output is disabled. When the input source signal has a rising edge, the rising edge deadband count starts and DBWxB output is disabled immediately. When the rising edge deadband delay is reached, DBWxA output is enabled. DBWDB0 and DBWDB1 registers are used to set the duration of the input source signal rising along the dead interval(0~63).

The DBWxB output is delayed when DBWxA output is disabled. When the input source signal has a falling edge, the falling edge deadband count starts and DBWxA output is disabled immediately. When the falling edge deadband delay is reached, DBWxB output is enabled. DBWDB0 and DBWDB1 registers are used to set the duration of the input source signal falling along the dead interval(0~63).

Deadband always stop count at falling edge of input source signal, a count of 0 indicates that there is no deadband time. If the input source signal does not appear long enough to complete the counting, no output will be generated on the corresponding output.

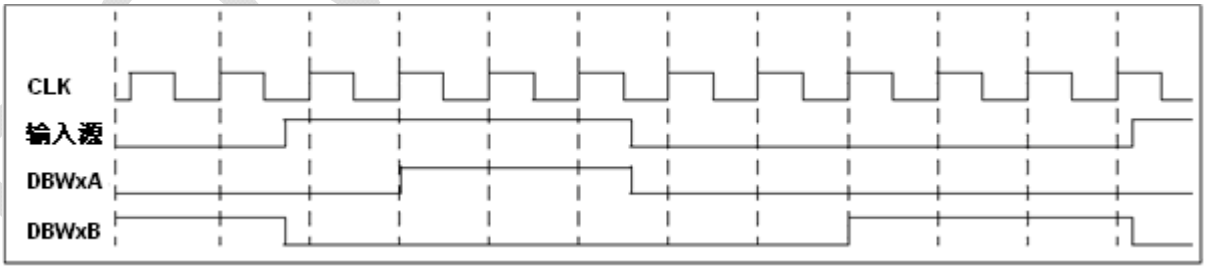


Figure 20-2 Deadband waveform (GxDBM=00H, DBWDB0=01H, DBWDB1=02H)

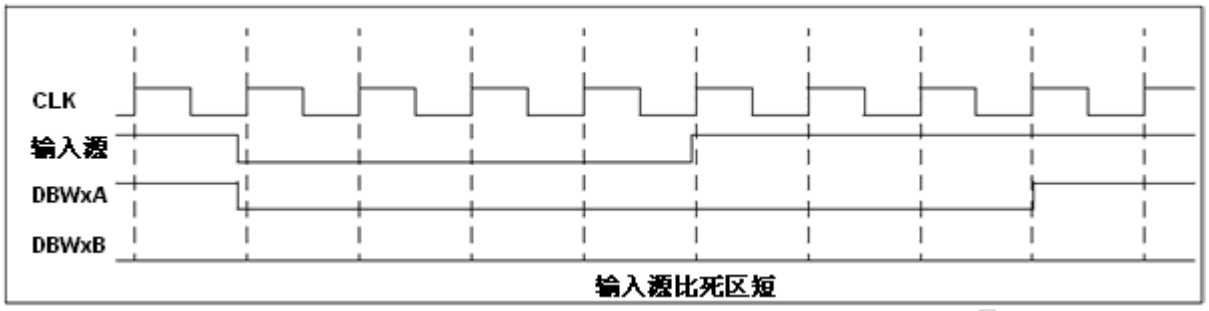


Figure 20-3 Deadband waveform(input sorce short deadband)(GxDBM=00H, DBWDB0=03H, DBWDB1=04H)

20.4 Automatic shutdown

Automatic shutdown is a method that uses a specific rewriting signal to immediately rewrite DBW output level, so as to safely shutdown the circuit. The shutdown state can be cleared automatically or kept until the software cleared. There are two shutdown methods: software shutdown and external input shutdown.

GxASE can be configured by software to force DBW to enter the shutdown state. When automatic restart is disabled, GxASE will keep the shutdown state as long as it is set to 1. when automatic restart is enabled, GxASE will be automatically cleared and continue to work when the next rising edge event occurs.

External input shutdown provides the fastest way to safety shutdown DBW in case of failure conditions. When any selected shutdown input becomes effective, DBW output immediately changes to the selected level without any software delay. Any combination of the two input sources ‘comparator ACMP’ and ‘external input DBWxIN’ can be selected to produce a shutdown condition. The shutdown input is level sensitive, so as long as the shutdown input level is present, the shutdown state cannot be removed unless automatic shutdown is disabled.

After an automatic shutdown event, two methods can be used to restore work: software control, automatic restart. The restart method is configured by the GxARSEN.

When GxARSEN is cleared, the DBW must be restarted using software after the automatic shutdown event. Clearing the shutdown input log requires all selected shutdown inputs to be low, otherwise GxASE will be set to 1. The off state level remains in effect until the first rising edge event occurs after GxASE is cleared, and the DBW resumes.

When GxARSEN is set to 1, DBW restarts automatically from the automatic shutdown state. When the source becomes low, GxASE will automatically clear to 0, and the off state level remains in effect until the first rising edge event occurs after GxASE is cleared to 0, and DBW will continue to operate.

Note: polarity control does not affect the level selected in the off state.

20.5 DBW configuration

The following steps show how to configure DBW correctly to ensure synchronization starts:

1. Clear GxEN
2. Set DBWDB0 and DBWDB1 register dead time
3. Set GxDBM register dead time select mode
4. Set DBWxCON2 automatic shutdown register and select the shutdown source
5. Set DBWxCON1 off status register and set the two outputs as the required level
6. Set GXASE to 1, clear GxARSEN
7. Configure GxIS and select the input source
8. Configure DBWxCON0 select the clock source (note the selection of PWM clock source), the output polarity
9. Set GxEN is 1
10. If restart automatically, set GxARSEN to 1, GxASE will be cleared automatically, otherwise start DBW by clear GxASE.

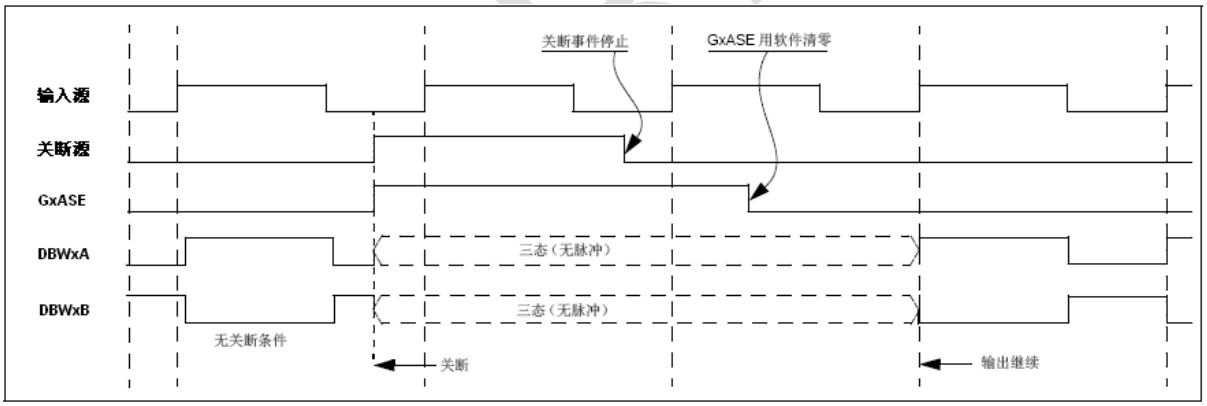


Figure 20-4 Shutdown fuction when automatic restart disenable

(GxARSEN=0, GxASDLA=01, GxASDLB=01)

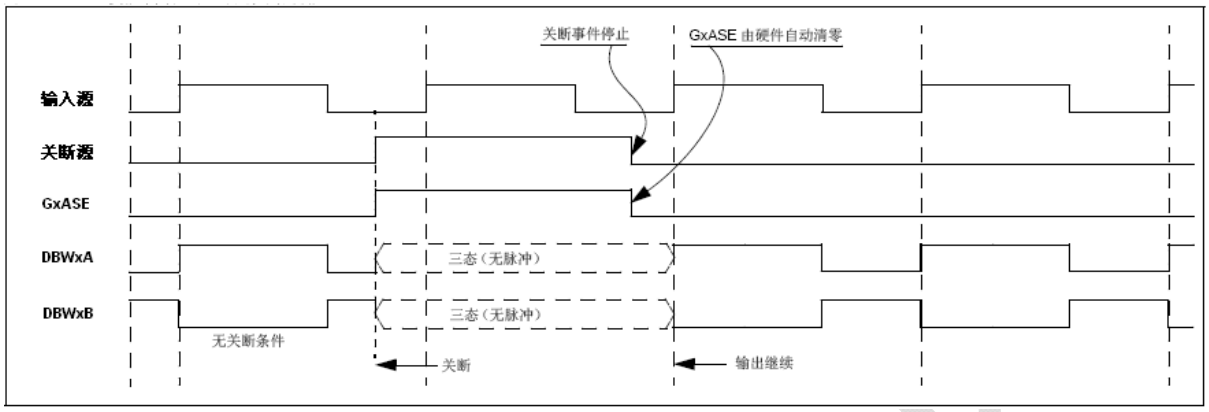


Figure 20-5 Shutdown function when automatic restart enable

(GxARSEN=1, GxASDLA=01, GxASDLB=01)

20.6 Register Definition

20.6.1 DBW Deadband Control Register 0–DBWDB0

Table 20-1 DBWDB0 Register (C1h)

Bit	Symbol	Description	Type	Reset
dbwdb0.7~6	-	Reserved	R	2'b0h
dbwdb0.5~0	-	DBW deadband control register 0	R/W	6'b0h

20.6.2 DBW Deadband Control Register 1–DBWDB1

Table 20-2 DBWDB0 Register (C2h)

Bit	Symbol	Description	Type	Reset
dbwdb1.7~6	-	Reserved	R	2'b0h
dbwdb1.5~0	-	DBW deadband control register 1	R/W	6'b0h

20.6.3 DBW Control Register–DBW0CON0

Table 20-2 DBW0CON0 Register (C3h)

Bit	Symbol	Description	Type	Reset
dbwcon0.7	G1EN	**DBW1 enable**	R/W	0

Bit	Symbol	Description	Type	Reset
		1 = enable module 0 = disable module		
dbwcon0.6	G1POLB	**DBW1B output polarity** 1 = output polarity toggled 0 = output polarity does not toggled	R/W	0
dbwcon0.5	G1POLA	**DBW1A output polarity** 1 = output polarity toggled 0 = output polarity does not toggled	R/W	0
dbwcon0.4	G1CS	**DBW1 clock source selection** 1 = GxIS select PWM clock 0 = CLKPER	R/W	0
dbwcon0.3	G0EN	**DBW0 enable** 1 = enable module 0 = disenable module	R/W	0
dbwcon0.2	G0POLB	**DBW0B output polarity** 1 = output polarity toggled 0 = output polarity does not toggled	R/W	0
dbwcon0.1	G0POLA	**DBW0A output polarity** 1 = output polarity toggled 0 = output polarity does not toggled	R/W	0
dbwcon0.0	G0CS	**DBW0 clock source selection** 1 = GxIS select PWM clock 0 = CLKPER	R/W	0

20.6.4 DBW Control Register–DBW0CON1

Table 20-3 DBW0CON1 Register (C4h)

Bit	Symbol	Description	Type	Reset
dbw0con1.7	G0ASDLB.1	**DBW0B DBW0 shutdown state**	R/W	0
dbw0con1.6	G0ASDLB.0	When automatic shutdown event occur (G0ASE = 1): 11 = DBW0B pin is driven to 1, regardless of the G0POLB setting. 10 = DBW0B pin is driven to 0, regardless of the G0POLB setting. 01 = DBW0B pin is tri-state 00 = After selected deadband interval, DBW0B pin is driven to its invalid state. The output polarity still controlled by G0POLB.	R/W	0
dbw0con1.5	G0ASDLA.1	**DBW0A DBW0 shutdown state**	R/W	0
dbw0con1.4	G0ASDLA.0	When automatic shutdown event occur (G0ASE = 1):	R/W	0

Bit	Symbol	Description	Type	Reset
		11 = DBW0A pin is driven to 1, regardless of the G0POLB setting. 10 = DBW0A pin is driven to 0, regardless of the G0POLB setting. 01 = DBW0A pin is tri-state 00 = After selected deadband interval, DBW0A pin is driven to its invalid state. The output polarity still controlled by G0POLA.		
dbw0con1.3	G0IS.3	**DBW0 input source selection** 0000 = ACMP1 0001 = PWM0 0010 = PWM1 0011 = PWM2 0100 = PWM3 0101 = PWM4 0110 = PWM5 0111 = DBW input 1000 = ACMP2(RSV) ---RSV reserved--- 1111 = T2CPO(PWM)	R/W	0
dbw0con1.2	G0IS.2		R/W	0
dbw0con1.1	G0IS.1		R/W	0
dbw0con1.0	G0IS.0		R/W	0

20.6.5 DBW Control Register–DBW0CON2

Table 20-4 DBW0CON2 Register (C5h)

Bit	Symbol	Description	Type	Reset
dbw0con2.7	G0ASE	**DBW0 automatic shutdown event status** 1 = automatic shutdown event occur 0 = no automatic shutdown event occur	R/W	0
dbw0con2.6	G0ARSEN	**DBW0 automatic restart enable** 1 = enable automatic restart 0 = disable automatic restart	R/W	0
dbw0con2.5	G0DBM.1	**DBW0 deadband time mode setting**	R/W	0
dbw0con2.4	G0DBM.0	0x = the before deadband of DBW0 set by DBWDB0, after deadband of DBW0 set by DBWDB1; 10 = the before and after deadband of DBW0 both set by DBWDB0; 11 = the before and after deadband of DBW0 both set by DBWDB0;	R/W	0
dbw0con2.3	-	-	R	0
dbw0con2.2	G0ASDSC	**DBW0 automatic shutdown based on comparator**	R/W	0

Bit	Symbol	Description	Type	Reset
		ACMP enable 1 = shutdown when comparator ACMP output ACMP_OUT_sync is high level; 0 = the output of comparator ACMP has no effect on shutdown		
dbw0con2.1	G0ASDSPPS	**DBW0 input pin enable** 1 = shutdown when DBW0 input pin (DBW0IN) is high level 0 = DBW0 input pin(DBW0IN) signal has no effect on shutdown	R/W	0
dbw0con2.0	G0ADOEN	**DBW0A direct output pin enable** 1 = direct output to DBW0A pin 0 = output to original function output pin	R/W	0

20.6.6 DBW Control Register–DBW1CON1

Table 20-6 DBW1CON1 Register (C6h)

Bit	Symbol	Description	Type	Reset
dbw1con1.7	G1ASDLB.1	**DBW1B DBW1 shutdown state**	R/W	0
dbw1con1.6	G1ASDLB.0	When automatic shutdown event occur (G1ASE = 1): 11 = DBW1B pin is driven to 1, regardless of the G1POLB setting. 10 = DBW1B pin is driven to 0, regardless of the G1POLB setting. 01 = DBW1B pin is tri-state 00 = After selected deadband interval, DBW1B pin is driven to its invalid state. The output polarity still controlled by G1POLB.	R/W	0
dbw1con1.5	G1ASDLA.1	**DBW1A DBW1 shutdown state**	R/W	0
dbw1con1.4	G1ASDLA.0	When automatic shutdown event occur (G1ASE = 1): 11 = DBW1A pin is driven to 1, regardless of the G1POLB setting. 10 = DBW1A pin is driven to 0, regardless of the G1POLB setting. 01 = DBW1A pin is tri-state 00 = After selected deadband interval, DBW1A pin is driven to its invalid state. The output polarity still controlled by G1POLA.	R/W	0
dbw1con1.3	G1IS.3	**DBW1 input source selection**	R/W	0
dbw1con1.2	G1IS.2	0000 = ACMP1	R/W	0

Bit	Symbol	Description	Type	Reset
dbw1con1.1	G1IS.1	0001 = PWM0	R/W	0
dbw1con1.0	G1IS.0	0010 = PWM1 0011 = PWM2 0100 = PWM3 0101 = PWM4 0110 = PWM5 0111 = DBW input 1000 = ACMP2(RSV) ---RSV reserved--- 1111 = T2CPO(PWM)	R/W	0

20.6.7 DBW Control Register–DBW1CON2

Table 20-7 DBW0CON2 Register (C7h)

Bit	Symbol	Description	Type	Reset
dbw1con2.7	G1ASE	**DBW1 automatic shutdown event status** 1 = automatic shutdown event occur 0 = no automatic shutdown event occur	R/W	0
dbw1con2.6	G1ARSEN	**DBW1 automatic restart enable** 1 = enable automatic restart 0 = disable automatic restart	R/W	0
dbw1con2.5	G1DBM.1	**DBW1 deadband time mode setting** 0x = the before deadband of DBW1 set by DBWDB1, after deadband of DBW1 set by DBWDB1; 10 = the before and after deadband of DBW1 both set by DBWDB1; 11 = the before and after deadband of DBW1 both set by DBWDB1;	R/W	0
dbw1con2.4	G1DBM.0		R/W	0
dbw1con2.3	-	-	R	0
dbw1con2.2	G1ASDSC1	**DBW1 automatic shutdown based on comparator ACMP enable** 1 = shutdown when comparator ACMP output ACMP_OUT_sync is high level; 0 = the output of comparator ACMP has no effect on shutdown	R/W	0
dbw1con2.1	G1ASDSPPS	**DBW1 input pin enable** 1 = shutdown when DBW1 input pin (DBW1IN) is high level 0 = DBW1 input pin(DBW1IN) signal has no effect on shutdown	R/W	0

Bit	Symbol	Description	Type	Reset
dbw1con2.0	G1ADOEN	**DBW1A direct output pin enable** 1 = direct output to DBW1A pin 0 = output to original function output pin	R/W	0

20.6.8 DBW Control Register–DBW2CON0

Table 20-8 DBW2CON0 Register (BBh)

Bit	Symbol	Description	Type	Reset
dbw2con0.7	-	-	R	0
dbw2con0.6	-	-	R	0
dbw2con0.5	-	-	R	0
dbw2con0.4	-	-	R	0
dbw2con0.3	G2EN	**DBW2 enable** 1 = enable module 0 = disenable module	R/W	0
dbw2con0.2	G2POLB	**DBW2B output polarity** 1 = output polarity toggled 0 = output polarity does not toggled	R/W	0
dbw2con0.1	G2POLA	**DBW2A output polarity** 1 = output polarity toggled 0 = output polarity does not toggled	R/W	0
dbw2con0.0	G2CS	**DBW2 clock source selection** 1 = GxIS select PWM clock 0 = CLKPER	R/W	0

20.6.9 DBW Control Register–DBW2CON1

Table 20-9 DBW2CON1 Register (BCh)

Bit	Symbol	Description	Type	Reset
dbw2con1.7	G2ASDLB.1	**DBW2B DBW2 shutdown state**	R/W	0
dbw2con1.6	G2ASDLB.0	When automatic shutdown event occur (G2ASE = 1): 11 = DBW2B pin is driven to 1, regardless of the G2POLB setting. 10 = DBW2B pin is driven to 0, regardless of the G2POLB setting. 01 = DBW2B pin is tri-state 00 = After selected deadband interval, DBW2B pin is driven to its invalid state. The output polarity still	R/W	0

Bit	Symbol	Description	Type	Reset
		controlled by G2POLB.		
dbw2con1.5	G2ASDLA.1	**DBW2A DBW2 shutdown state**	R/W	0
dbw2con1.4	G2ASDLA.0	When automatic shutdown event occur (G2ASE = 1): 11 = DBW2A pin is driven to 1, regardless of the G2POLB setting. 10 = DBW2A pin is driven to 0, regardless of the G2POLB setting. 01 = DBW2A pin is tri-state 00 = After selected deadband interval, DBW2A pin is driven to its invalid state. The output polarity still controlled by G2POLA.	R/W	0
dbw2con1.3	G2IS.3	**DBW2 input source selection**	R/W	0
dbw2con1.2	G2IS.2	0000 = ACMP1	R/W	0
dbw2con1.1	G2IS.1	0001 = PWM0	R/W	0
dbw2con1.0	G2IS.0	0010 = PWM1 0011 = PWM2 0100 = PWM3 0101 = PWM4 0110 = PWM5 0111 = DBW input 1000 = ACMP2(RSV) ---RSV reserved--- 1111 = T2CPO(PWM)	R/W	0

20.6.10 DBW Control Register–DBW2CON2

Table 20-10 DBW2CON2 Register (BDh)

Bit	Symbol	Description	Type	Reset
dbw2con2.7	G2ASE	**DBW2 automatic shutdown event status** 1 = automatic shutdown event occur 0 = no automatic shutdown event occur	R/W	0
dbw2con2.6	G2ARSEN	**DBW2 automatic restart enable** 1 = enable automatic restart 0 = disable automatic restart	R/W	0
dbw2con2.5	G2DBM.1	**DBW2 deadband time mode setting**	R/W	0
dbw2con2.4	G2DBM.0	0x = the before deadband of DBW2 set by DBWDB2, after deadband of DBW2 set by DBWDB1; 10 = the before and after deadband of DBW2 both set by DBWDB0; 11 = the before and after deadband of DBW2 both set	R/W	0

Bit	Symbol	Description	Type	Reset
		by DBWDB0;		
dbw2con2.3	-	-	R	0
dbw2con2.2	G2ASDSC1	**DBW2 Automatic shutdown based on comparator ACMP enable** 1 = shutdown when comparator ACMP output ACMP_OUT_sync is high level; 0 = the output of comparator ACMP has no effect on shutdown	R/W	0
dbw2con2.1	G2ASDSPPS	**DBW2 input pin enable** 1 = shutdown when DBW2 input pin (DBW2IN) is high level 0 = DBW2 input pin(DBW2IN) signal has no effect on shutdown	R/W	0
dbw2con2.0	G2ADOEN	**DBW2A direct output pin enable** 1 = direct output to DBW2A pin 0 = output to original function output pin	R/W	0

21 BEEPER

21.1 Overview

1KHz, 2KHz and 4KHz beeper signal can be generated by LIRC (32KHz).

21.2 Register Definition

21.2.1 Beeper Control Register–BEEPER

Table 21-1 BEEPER Register (91h)

Bit	Symbol	Description	Type	Reset
beeper.7	BEEPEN	**Beeper enable** 0：disable beeper function 1：enable beeper function This bit set and clear by software, enable beeper function.	R/W	0
beeper.6	BEEPSEL1	**Beeper frequency selection** 00: output fLS/(8 x BEEPDIV) kHz 01: output fLS/(4 x BEEPDIV) kHz 1x: output fLS/(2 x BEEPDIV) kHz	R/W	0
beeper.5	BEEPSEL0		R/W	0
beeper.4	BEEPDIV4	**Beeper prescaler selection** 00h: BEEPDIV = 2 01h: BEEPDIV = 3 ... 0Eh: BEEPDIV = 16 0Fh: BEEPDIV = 17 .... 1Eh: BEEPDIV = 32 Those bits set and clear by software, set beeper prescale factor BEEPDIV. Note: this register cannot set its initial reset value (0x1F).	R/W	1
beeper.3	BEEPDIV3		R/W	1
beeper.2	BEEPDIV2		R/W	1
beeper.1	BEEPDIV1		R/W	1
beeper.0	BEEPDIV0		R/W	1

22 UART0

The Serial provides a flexible full-duplex synchronous/asynchronous receiver/transmitter. It can operate in four modes (one synchronous and three asynchronous). The Serial is buffered at the receive side, i.e. it can revive new data while the previously received is not damaged in the receive register until the completion of the 2nd transfer. The Serial is fully compatible with the standard 8051 serial channel.

The transmit register and the receive buffer are both addressed as S0BUF Special Function Register. However any write to S0BUF will be to the transmit register, while a read from S0BUF will be from the receiver buffer register.

22.1 Mode 0

In mode 0 the Serial Port 0 operates as synchronous transmitter/receiver. The TXD0 outputs the shift clock. The RXD0 outputs data and inputs data. 8 bits are transmitted with LSB first. The baud rate is fixed at 1/12 of the main clock frequency. Reception is started by setting the S0CON.REN0, and clearing the S0CON.RI0. Transmission is started by writing data to S0BUF register.

22.2 Mode 1

In mode 1 the Serial Port 0 operates as asynchronous transmitter/receiver with 8 data bits and programmable baud rate. Additionally the baud rate can be doubled with the use of the T2MOD.S0BDD.

Transmission is started by writing to the S0BUF register. The TXD0 pin outputs data. Each transmit data is 10 bits: the first bit transmitted is a start bit (always 0), then 8 bits of data proceed, after which a stop bit (always 1) is transmitted.

The RXD0 pin inputs data. When reception starts, the Serial Port synchronizes with the falling edge detected at pin RXD0. Input data are available after completion of the reception in the S0BUF register, and the value of stop bit is available as the S0CON.RB80. During the reception, the S0BUF and S0CON.RB80 remain unchanged until the completion.

22.3 Mode 2

In mode 2 the Serial Port operates as asynchronous transmitter/receiver with 9 data bits, and baud rate fixed to 1/32 or 1/64 of system clock, depending on the setting of T2MOD.S0BDD.

Transmission is started by writing to the S0BUF register. The TXD0 pin outputs data. The first bit transmitted is a start bit (always 0), then 9 bits of data proceed where the 9th is taken from bit S0CON.TB80 after which a stop bit (always 1) is transmitted.

The RXD0 pin inputs data. When reception starts, the Serial Port synchronizes with the falling edge detected at pin RXD0. Input data are available after completion of the reception in the S0BUF register, and the 9th bit is available as the S0CON.RB80. During the reception, the S0BUF and S0CON.RB80 remain unchanged until the completion.

22.4 Mode 3

The only difference between Mode 2 and Mode 3 is that in Mode 3 Timer 1 can be used to specify the baud rate.

In mode 3 the Serial Port operates as asynchronous transmitter/receiver with 9 data bits and programmable baud rate. Additionally the baud rate can be doubled with the use of the T2MOD.S0BDD.

Transmission is started by writing to the S0BUF register. The TXD0 pin outputs data. The first bit transmitted is a start bit (always 0), then 9 bits of data proceed where the 9th is taken from bit S0CON.TB80, after which a stop bit (always 1) is transmitted.

The RXD0 pin inputs data. When reception starts, the Serial Port synchronizes with the falling edge detected at pin RXD0. Input data are available after completion of the reception in the S0BUF register, and the 9th bit is available as the S0CON.RB80. During the reception, the S0BUF and S0CON.RB80 remain unchanged until the completion.

22.5 Baud Rate

The baud rate for Serial Port working in mode 1 or mode 3:

When T2MOD.S0BDS=0, baud rate is:

((2^S0BDD) * Fclk / 32) * Timer1_OverFlow_Rate

When T2MOD.S0BDS=1, baud rate is:

((2^S0BDD) * Fclk) / (64 * ((2^10) - {S0BDH,S0BDL}))

22.6 The Serial Port 0 Multiprocessor Communication

The feature of receiving 9 bits in Modes 2 and 3 of Serial Interface 0 can be used for multiprocessor communication.

When the S0CON.S0M2 is set, the receive interrupt is generated only when the 9th received bit (S0CON.RB80) is 1. Otherwise, no interrupt is generated upon reception.

To utilize this feature to multiprocessor communication, the slave processors have their S0CON.S0M2 bit set to 1. The master processor transmits the slave's address, with the 9th bit set to 1, causing reception interrupt in all of the slaves. The slave processors' software compares the received byte with their network address. If there is a match, the addressed slave clears its

S0CON.S0M2 and the rest of the message is transmitted from the master with the 9th bit set to 0. The other slaves keep their S0CON.S0M2 set to 1 so that they ignore the rest of the message sent by the master.

22.7 Register Definition

22.7.1 Serial Port 0 Control Register – S0CON

Table 22-1 S0CON Register (98h)

Bit	Symbol	Description	Type	Reset
s0con.7	s0m0	**Serial Port 0 mode select**	R/W	0
s0con.6	s0m1		R/W	0
s0con.5	s0m2	**Multiprocessor communication enable**	R/W	0
s0con.4	ren0	**Serial Port 0 reception enable** If set HIGH serial reception at Serial Port is enabled. Otherwise serial reception at Serial Port is disabled.	R/W	0
s0con.3	tb80	**Serial Port 0 transmitter bit 8** This bit is used while transmitting data through Serial Port 0 in Modes 2 and 3. The state of this bit corresponds with the state of the 9th transmitted bit (e.g. parity check or multiprocessor communication). It is controlled by software.	R/W	0
s0con.2	rb80	**Serial Port 0 received bit 8** This bit is used while receiving data through Serial Port 0 in Modes 2 and 3. It reflects the state of the 9th received bit. In Mode 1, if multiprocessor communication is enabled (sm2 = 0), this bit is the stop bit that was received. In Mode 0 this bit is not used.	R/W	0
s0con.1	ti0	**Serial Port 0 transmit interrupt flag** It indicates completion of a serial transmission at Serial Port. It is set by hardware at the end of bit 8 in mode 0 or at the beginning of a stop bit in other modes. It must be cleared by software.	R/W	0
s0con.0	ri0	**Serial Port 0 receive interrupt flag** It is set by hardware after completion of a serial reception at Serial Port 0. It is set by hardware at the end of bit 8 in mode 0 or in the middle of a stop bit in other modes. It must be cleared by software.	R/W	0

Table 22-2 Serial Port modes and Baud Rates

sm0	sm1	Mode	Description	Baud Rate	
0	0	Mode 0	Shift register	Fsys/12	
0	1	Mode 1	8-bit UART	Timer 1 overflow or S0BDH/L	
1	0	Mode 2	9-bit UART	Depends on T2MOD.S0BDD	
				smod	Baud Rate
				0	Fsys/64
				1	Fsys/32
1	1	Mode 3	9-bit UART	Timer 1 overflow or S0BDH/L	

22.7.2 Serial Port 0 Data Buffer – S0BUF

Table 22-3 S0BUF Register (99h)

Bit	Symbol	Description	Type	Reset
s0buf.7~0	-	Serial port 0 data buffer	R/W	00h

22.7.3 Serial Port 0 Baud Rate Register – S0BDH/S0BDL

Table 22-4 S0BDH Register (9Bh)

Bit	Symbol	Description	Type	Reset
s0bdh.7~0	-	Serial port 0 baud rate high 2bit	R/W	03h

Table 22-5 S0BDL Register (9Ah)

Bit	Symbol	Description	Type	Reset
s0bdl.7~0	-	Serial port 0 baud rate low 8bit	R/W	D9h

23 UART1

The Serial provides a flexible full-duplex synchronous/asynchronous receiver/transmitter. It can operate in two modes. The Serial is buffered at the receive side, i.e. it can revive new data while the previously received is not damaged in the receive register until the completion of the 2nd transfer.

The transmit register and the receive buffer are both addressed as S1BUF Special Function Register. However any write to S1BUF will be to the transmit register, while a read from S1BUF will be from the receiver buffer register.

23.1 Mode 1

In mode 1 the Serial Port 1 operates as asynchronous transmitter/receiver with 8 data bits and programmable baud rate, depending on S1BDH/S1BDL register.

Transmission is started by writing to the S1BUF register. The TXD1 pin outputs data. Each transmit data is 10 bits: The first bit transmitted is a start bit (always 0), then 8 bits of data proceed (LSB first), after which a stop bit (always 1) is transmitted.

The RXD1 pin inputs data. When reception starts, the Serial Port synchronizes with the falling edge detected at pin RXD1. Input data are available after completion of the reception in the S1BUF register, and the value of stop bit is available as the S1CON.RB81. During the reception, the S1BUF and S1CON.RB81 remain unchanged until the completion.

23.2 Mode 2

In mode 2 the Serial Port 1 operates as asynchronous transmitter/receiver with 9 data bits and programmable baud rate, depending on S1BDH/S1BDL register.

Transmission is started by writing to the S1BUF register. The TXD1 pin outputs data. Each transmit data is 10 bits: The first bit transmitted is a start bit (always 0), then 9 bits of data proceed (LSB first) where the 9th is taken from bit S1CON.TB81 after which a stop bit (always 1) is transmitted.

The RXD1 pin inputs data. When reception starts, the Serial Port synchronizes with the falling edge detected at pin RXD1. Input data are available after completion of the reception in the S1BUF register, and the 9th bit is available as the S1CON.RB81. During the reception, the S1BUF and S1CON.RB81 remain unchanged until the completion.

23.3 Baud Rate

The baud rate for Serial Port 1:

Fclk / (32 * ((2^10) - {S0BDH,S0BDL}))

23.4 The Serial Port 1 Multiprocessor Communication

The feature of receiving 9 bits in mode 2 of Serial Port 1 can be used for multiprocessor communication.

When the S1CON.S1M2 is set, the receive interrupt is generated only when the 9th received bit (S1CON.RB81) is 1. Otherwise, no interrupt is generated upon reception.

To utilize this feature to multiprocessor communication, the slave processors have their S1CON.S1M2 bit set to 1. The master processor transmits the slave's address, with the 9th bit set to 1, causing reception interrupt in all of the slaves. The slave processors' software compares the received byte with their network address. If there is a match, the addressed slave clears its S1CON.S1M2 and the rest of the message is transmitted from the master with the 9th bit set to 0. The other slaves keep their S1CON.S1M2 set to 1 so that they ignore the rest of the message sent by the master.

23.5 Register Definition

23.5.1 Serial Port 1 Control Register – S1CON

Table 23-1 S1CON Register (9Fh)

Bit	Symbol	Description	Type	Reset
s1con.7	s1m0	**Serial Port 1 mode select** 0: Mode 2, 9-bit UART 1: Mode 1, 8-bit UART	R/W	0
s1con.6	-	-	R/W	0
s1con.5	s1m2	**Serial Port 1 Multiprocessor communication enable**	R/W	0
s1con.4	ren1	**Serial Port 1 Serial reception enable** 0: enabled. 1: disabled.	R/W	0
s1con.3	tb81	**Serial Port 1 Transmitter bit 8** This bit is used while transmitting data through Serial Port in Modes 2. The state of this bit corresponds with the state of the 9th transmitted bit (e.g. parity check or multiprocessor communication). It is controlled by software.	R/W	0
s1con.2	rb81	**Serial Port 1 Received bit 8** This bit is used while receiving data through Serial Port 1 in Modes 2. It reflects the state of the 9th received bit. In Mode 1, if multiprocessor communication is enabled (s1m2 = 0), this bit is the stop bit that was received.	R/W	0
s1con.1	ti1	**Serial Port 1 Transmit interrupt flag**	R/W	0

Bit	Symbol	Description	Type	Reset
		It indicates completion of a serial transmission at Serial Port. It is set by hardware at the beginning of a stop bit. It must be cleared by software.		
s1con.0	ri1	**Serial Port 1 Receive interrupt flag** It is set by hardware after completion of a serial reception at Serial Port 1. It is set by hardware at the end of reception or in the middle of a stop bit. It must be cleared by software.	R/W	0

23.5.2 Serial Port 1 Data Buffer – S1BUF

Table 23-2 S1BUF Register (9Ch)

Bit	Symbol	Description	Type	Reset
s1buf.7~0	-	Serial port 1 data buffer	R/W	00h

23.5.3 Serial Port 1 Baud Rate Register – S1BDH/S1BDL

Table 23-3 S1BDH Register (9Eh)

Bit	Symbol	Description	Type	Reset
s1bdh.7~0	-	Serial port 1 baud rate high 2bit	R/W	03h

Table 23-4 S1BDL Register (9Dh)

Bit	Symbol	Description	Type	Reset
s1bdl.7~0	-	Serial port 1 baud rate low 8bit	R/W	00h

24 SPI

The Serial Peripheral Interface (SPI) allows high-speed, full-duplex synchronous data transfer between the device and peripheral devices or between multiple microcontroller devices, including multiple masters and slaves on a single bus.

The SPI interface is often used to communicate with external peripheral devices such as RF transceiver, sensors, Flash or EEPROM memory devices etc. Originally developed by Motorola, the four line SPI interface is a synchronous serial data interface that has a relatively simple communication protocol simplifying the programming requirements when communicating with external hardware devices.

Although the SPI interface specification can control multiple slave devices from a single master, but this device provided only one SCSB pin. If the master needs to control multiple slave devices from a single master, the master can use I/O pin to select the slave devices.

24.1 SPI Interface

The SPI interface is a full duplex synchronous serial data link. It is a four line interface with pin names MISO, MOSI, SCK and SCSB. Pins MISO and MOSI are the Serial Data Input and Serial Data Output lines, SCK is the Serial Clock line and SCSB is the Slave Select line. As the SPI interface pins are pin-shared with normal I/O pins and with the I2C function pins. Communication between devices connected to the SPI interface is carried out in a slave/master mode with all data transfer initiations being implemented by the master. The Master also controls the clock signal. As the device only contains a single SCSB pin only one slave device can be utilized. The SCSB pin is controlled by software.

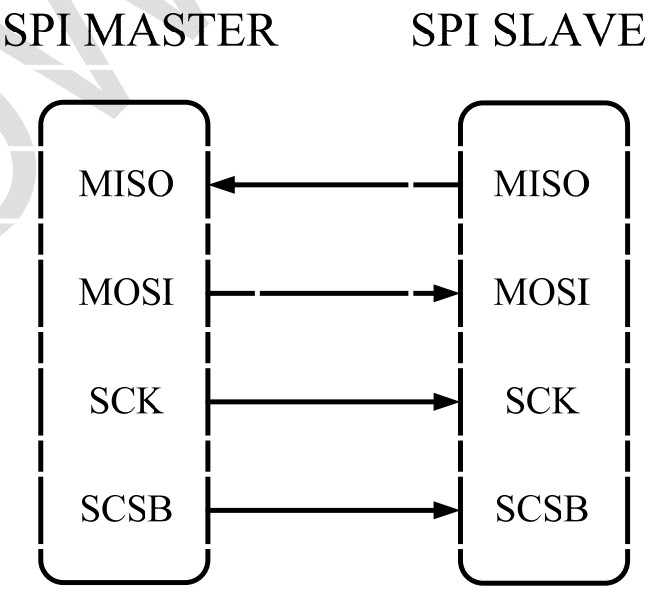


Figure 24-1 SPI Master/Slave Connection

24.2 SPI Communication

After the SPI interface is enabled by setting the SPCON.SPEN bit high, then in the Master Mode, when data is written to the SPDAT register, transmission/reception will begin simultaneously. When the data transfer is complete, the SPIF flag will be set automatically, but must be cleared using the application program.

In the Slave Mode, when the clock signal from the master has been received, any data in the SPDAT register will be transmitted and any data on the MISO pin will be shifted into the SPDAT register. The master should output an SCSB signal to enable the slave device before a clock signal is provided. The slave data to be transferred should be well prepared at the appropriate moment relative to the SCSB signal.

SPI communication timing waveform is shown as below:

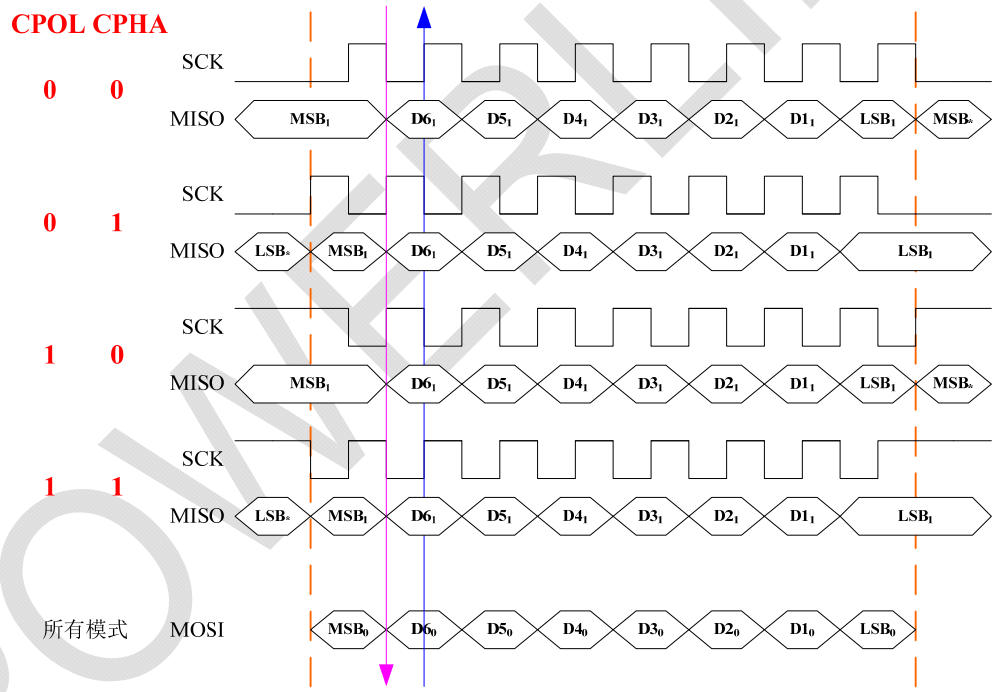


Figure 24-2 SPI bus protocol master transmission

When SPI is configured as master transmission data mode, SCSB is set to low level, SPI can perform continuous transmission.

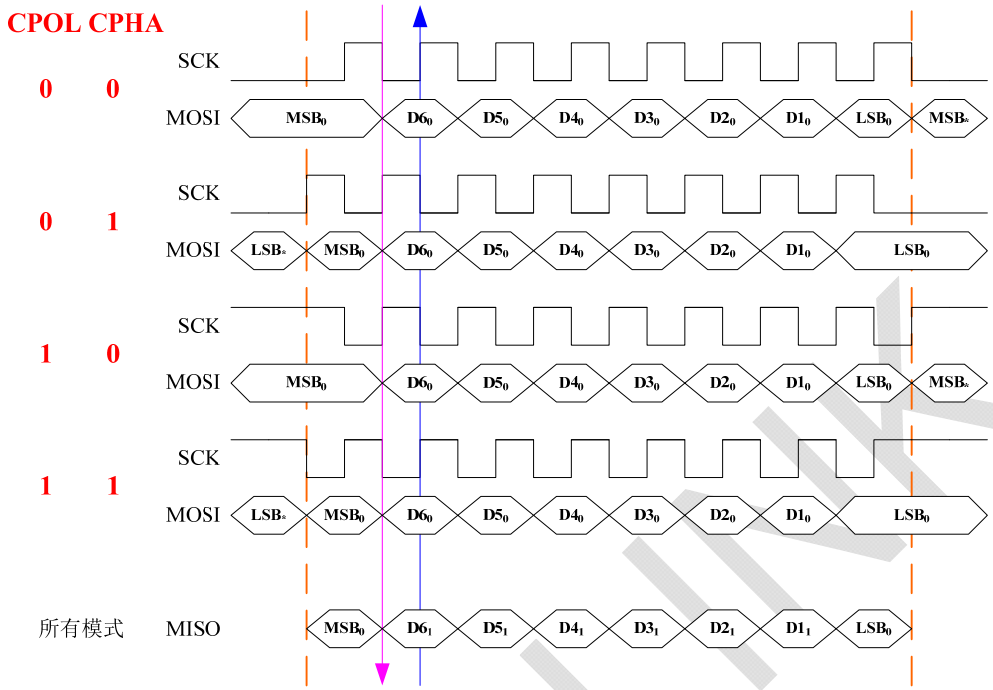


Figure 24-3 SPI bus protocol slave transmission

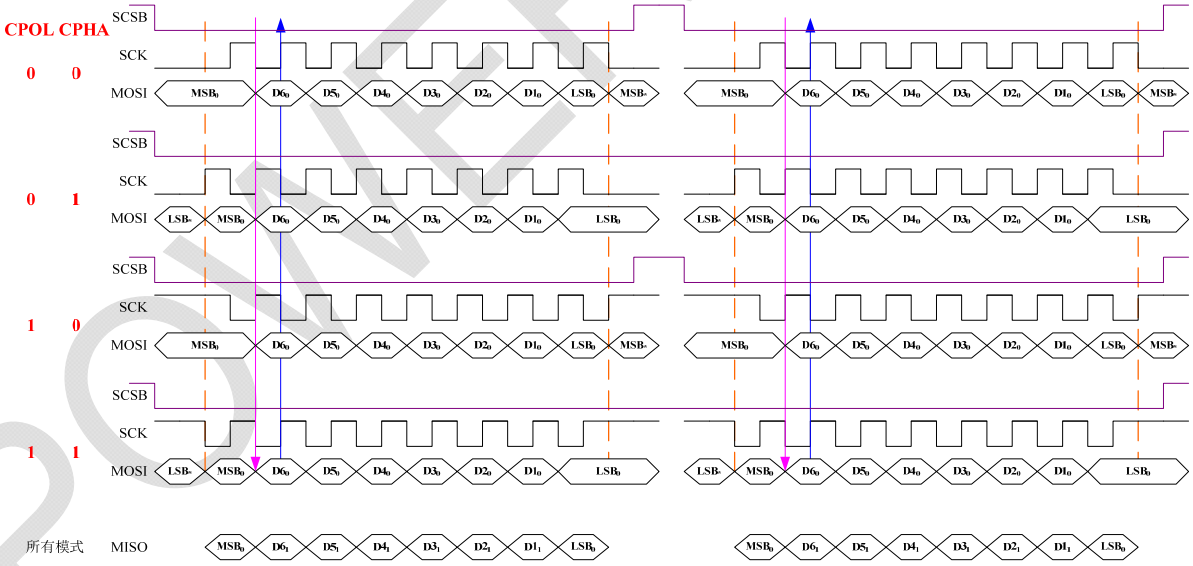


Figure 24-4 SPI bus protocol slave continuous transmission

When SPI is configured as slave mode, cpha is set to low level, after a data transmission, need to configure SCSB high level switch to low level again, SPI slave start next data transmission.

When SPI is configured as slave mode, cpha is set to high level, SCSB is set to low level, SPI can perform continuous transmission.

24.3 Register Definition

24.3.1 SPI Serial Peripheral Status Register – SPSTA

Table 24-1 SPSTA Register (B2h)

Bit	Symbol	Description	Type	Reset
spsta.7	spif	**Serial Peripheral Data Transfer Flag** Set by hardware upon data transfer completion. Cleared by reading the "spsta" register with the "spif" bit set, and then reading the "spdat" register.	R	0
spsta.6	wcol	**Write Collision Flag** Set by hardware upon write collision to "spdat". Cleared by an access to "spsta" register and an access to "spdat" register.	R	0
spsta.5	sserr	**Synchronous Serial Slave Error Flag** Set by hardware when "ssn" input is deasserted before the end of receive sequence. Cleared by disabling the SPI module (clearing "spen" bit in "spcon" register).	R	0
spsta.4	modf	**Mode Fault Flag** Set by hardware when the SCSB pin level is in conflict with actual mode of the SPI controller (configured as master while externally selected as slave). Cleared by hardware when the SCSB pin is at appropriate level. Can be also cleared by software by reading the "spsta" register with "modf" bit set.	R	0
spsta.3~0	-	-	R	4'b0

24.3.2 SPI Serial Peripheral Control Register – SPCON

Table 24-2 SPCON Register (B0h)

Bit	Symbol	Description	Type	Reset
spcon.7	spr2	**Serial Peripheral Rate 2** Together with "spr1" and "spr0" defines the clock rate in master mode.	R/W	0
spcon.6	spen	**Serial Peripheral Enable** When cleared disables the SPI interface. When set enables the SPI interface.	R/W	0

Bit	Symbol	Description	Type	Reset
spcon.5	ssdis	**SS Disable** When cleared enables the SCSB input in both Master and Slave modes. When set disables the SCSB input in both Master and Slave modes. In Slave mode, this bit has no effect if "cpha"=1. When "ssdis" is set, no "modf" interrupt request will be generated.	R/W	0
spcon.4	mstr	**Serial Peripheral Master** When cleared configures the SPI as a Slave. When set configures the SPI as a Master.	R/W	1
spcon.3	cpol	**Clock Polarity** When cleared, the SCK is set to 0 in idle state. When set, the SCK is set to 1 in idle state.	R/W	0
spcon.2	cpha	**Clock Phase** When cleared, data is sampled at first edge of SCK period. When set, data is sampled at second edge of SCK period. Note: when SPI is configured as slave mode, cpha is set to low level, SCSB is set to low level, data is sampled at first edge of SCK period, after a data transmission, spif is set to 1 by hardware, need to configure SCSB high level switch to low level again, SPI slave start next data transmission; If cpha is set to high level, SPI can perform continuous transmission.	R/W	1
spcon.1	spr1	**Serial Peripheral Rate** Together with "spr2" specify the serial clock rate in Master mode.	R/W	0
spcon.0	spr0		R/W	0

Table 24-3 Serial Peripheral Rate

spr2	spr1	spr0	Serial Peripheral Rate
0	0	0	Fclk/2
0	0	1	Fclk/4
0	1	0	Fclk/8
0	1	1	Fclk/16
1	0	0	Fclk/32
1	0	1	Fclk/64
1	1	0	Fclk/128
1	1	1	the master clock is not generated (when "cpol" = '1' SCK is high level, otherwise is low level

24.3.3 SPI Serial Peripheral Data Register – SPDAT

Table 24-4 SPDAT Register (B1h)

Bit	Symbol	Description	Type	Reset
spdat.7~0	-	SPI serial peripheral data	R/W	00h

25 I2C

The I2C interface is a two line low speed serial interface for synchronous serial data transfer, used to communicate with external peripheral devices such as RF transceiver, sensors, EEPROM memory etc. The advantage of only two lines for communication, relatively simple communication protocol and the ability to accommodate multiple devices on the same bus has made it an extremely popular interface type for many applications.

25.1 I2C Interface

The I2C serial interface is a two line interface, a serial data line, SDA, and serial clock line, SCL. As many devices may be connected together on the same bus, their outputs are both open drain types. For this reason it is necessary that external pull-high resistors are connected to these outputs. Note that no chip select line exists, as each device on the I2C bus is identified by a unique address which will be transmitted and received on the I2C bus.

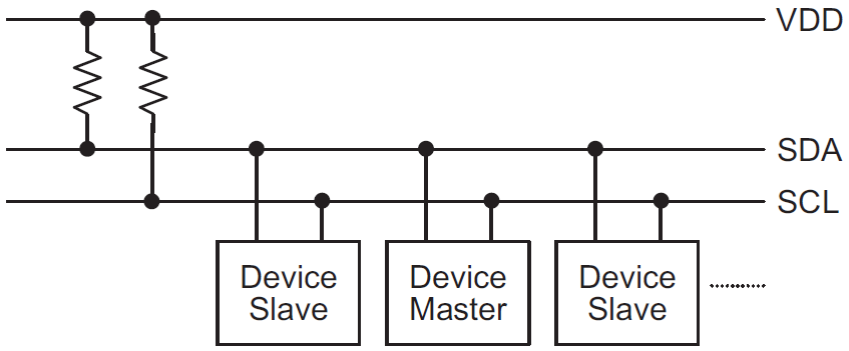


Figure 25-1 I2C Master Slave Bus Connection

25.2 I2C Communication

When two devices communicate with each other on the bidirectional I2C bus, one is known as the master device and one as the slave device. Both master and slave can transmit and receive data, however, it is the master device that has overall control of the bus. For these devices, which only operates in slave mode, there are two methods of transferring data on the I2C bus, the slave transmit mode and the slave receive mode. When the I2C device is activated, the pull-up resistance control function and SCL/SDA pin function still in effect, pull-up resistance function controlled by relevant pull-up resistance control register.

Communication on the I2C bus requires four separate steps, a START signal, a slave device address transmission, a data transmission and finally a STOP signal. When a START signal is placed on the I2C bus, all devices on the bus will receive this signal and be notified of the imminent arrival of data on the

bus. The first seven bits of the data will be the slave address with the first bit being the MSB.

Note: The START signal can only be generated by the master device connected to the I2C bus and not by the slave device. This START signal will be detected by all devices connected to the I2C bus. A START condition occurs when a high to low transition on the SDA line takes place when the SCL line remains high.

I2C communication timing waveform is shown as below:

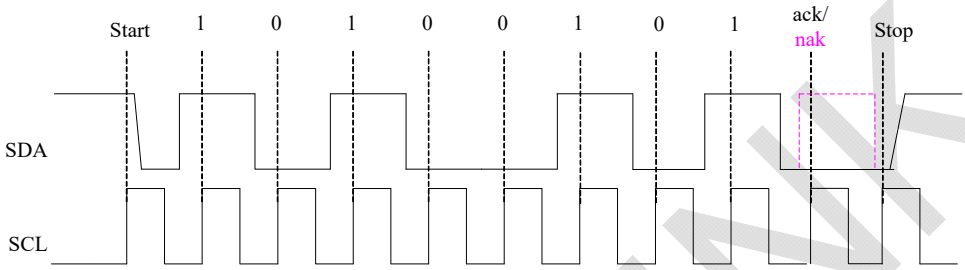


Figure 25-2 I2C bus protocol

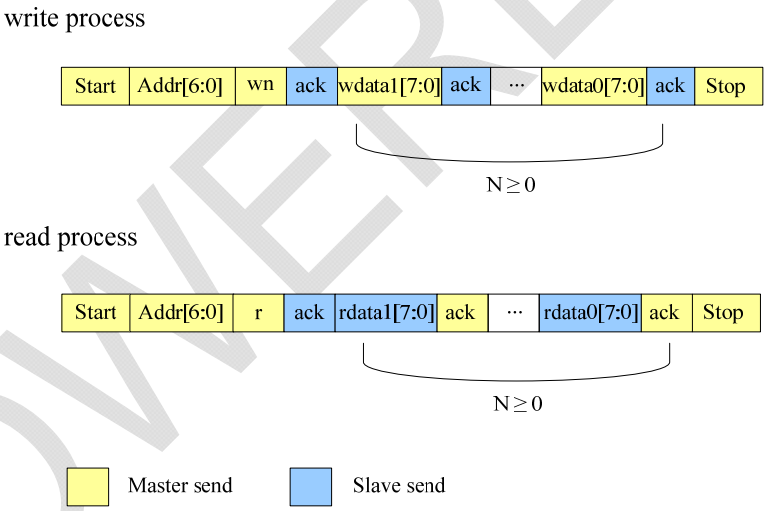


Figure 25-3 I2C communication timing waveform

25.3 Register Definition

25.3.1 I2C Status Register – I2CSTA

Table 25-1 I2CSTA Register (B6h)

Bit	Symbol	Description	Type	Reset
i2csta.7~3	-	**I2C Status Code**	R	F8h
i2csta.2~0	-	-	R	

25.3.2 I2C Control Register – I2CCON

Table 25-2 I2CCON Register (B7h)

Bit	Symbol	Description	Type	Reset
i2ccon.7	cr2	**Clock rate bit 2**	R/W	0
i2ccon.6	ens1	**I2C enable bit**	R/W	0
i2ccon.5	sta	**START Flag** When sta='1', the I2C component checks the I2C bus status and if the bus is free a START condition is generated.	R/W	0
i2ccon.4	sto	**STOP Flag** When sto='1' and I2C interface is in master mode, a STOP condition is transmitted to the I2C bus.	R/W	0
i2ccon.3	si	**Serial Interrupt Flag** The "si "is set by hardware when one of 25 out of 26 possible I2C states is entered. The only state that does not set the "si" is state F8h, which indicates that no relevant state information is available. The "si" flag must be cleared by software. In order to clear the "si" bit, '0' must be written to this bit. Writing a '1' to si bit does not change value of the "si".	R/W	0
i2ccon.2	aa	**Assert Acknowledge Flag** When aa='1', an "acknowledge" will be returned when: - the "own slave address" has been received - the general call address has been received while gc bit in i2caddr register was set - a data byte has been received while I2C was in master receiver mode - a data byte has been received while I2C was in slave receiver mode When aa='0', an "not acknowledge" will be returned when: - a data byte has been received while I2C was in master receiver mode - a data byte has been received while I2C was in slave receiver mode	R/W	0
i2ccon.1	cr1	**Clock rate bit 1**	R/W	0
i2ccon.0	cr0	**Clock rate bit 0**	R/W	0

This programmable clock pulse generator provides the “sclo” clock pulses when the I2C is in the master mode. The clock generator is suppressed when the I2C is in the slave mode.

The function of the clock generator is controlled by bits “cr0”, “cr1” and “cr2” of “i2ccon” register. The table below shows the possible rates of “clko” in the master mode.

The “bclk” input referenced in the table is connected to the Timer 1 overflow output. That means the baud rate of the I2C can be controlled by the Timer 1.

Table 25-3 I2CCON Clock Rate Control

cr2	cr1	cr0	Bit Frequency				CLK Divided
			4MHz	8MHz	12MHz	16MHz	
0	0	0	15.6	31	47	63	256
0	0	1	17.8	35.8	54	71	224
0	1	0	21	42	63	83	192
0	1	1	15	50	75	100	160
1	0	0	4.2	8.4	12.5	17	960
1	0	1	33.3	66.6	100	133	120
1	1	0	66.6	133.3	200	266	60
1	1	1	“bclk”(T1 overflow) input divided by 8				

25.3.3 I2C Address Register – I2CADR

Table 25-4 I2CADR Register (B4h)

Bit	Symbol	Description	Type	Reset
i2cadr.7~1	adr	**Own I2C slave address** (7 bit)	R/W	7’b0
i2cadr.0	gc	**General Call Address Acknowledge** If this bit is set, the general call address is recognized; otherwise it is ignored.	R/W	1’b0

25.3.4 I2C Data Register – I2CDAT

Table 25-5 I2CDAT Register (B5h)

Bit	Symbol	Description	Type	Reset
i2cdat.7~0	-	I2C data	R/W	00h

26 ADC&TSC

26.1 Overview

The 11 bits successive approximation ADC is built in the chip, which optimizes the performance and increases the application flexibility of ADC.

The chip supports the functions of ADC and temperature sensor, but just could be configured by CPU as one function separately at one time, since temperature sensor function need to use ADC module for calculating.

ADC function and temperature sensor function could only work in normal and IDLE mode, and the operation clock could be selected as 1/2/4/8/16/32/64/128 pre-scale of system clock.

In normal and IDLE mode, both system clock and 32KHz internal clock are always working. While only 32KHz clock is always working in low power mode, though system clock could be used when needed, for reduce the power consumption.

The block diagram of ADC&TSC function is shown as Figure 26-1：

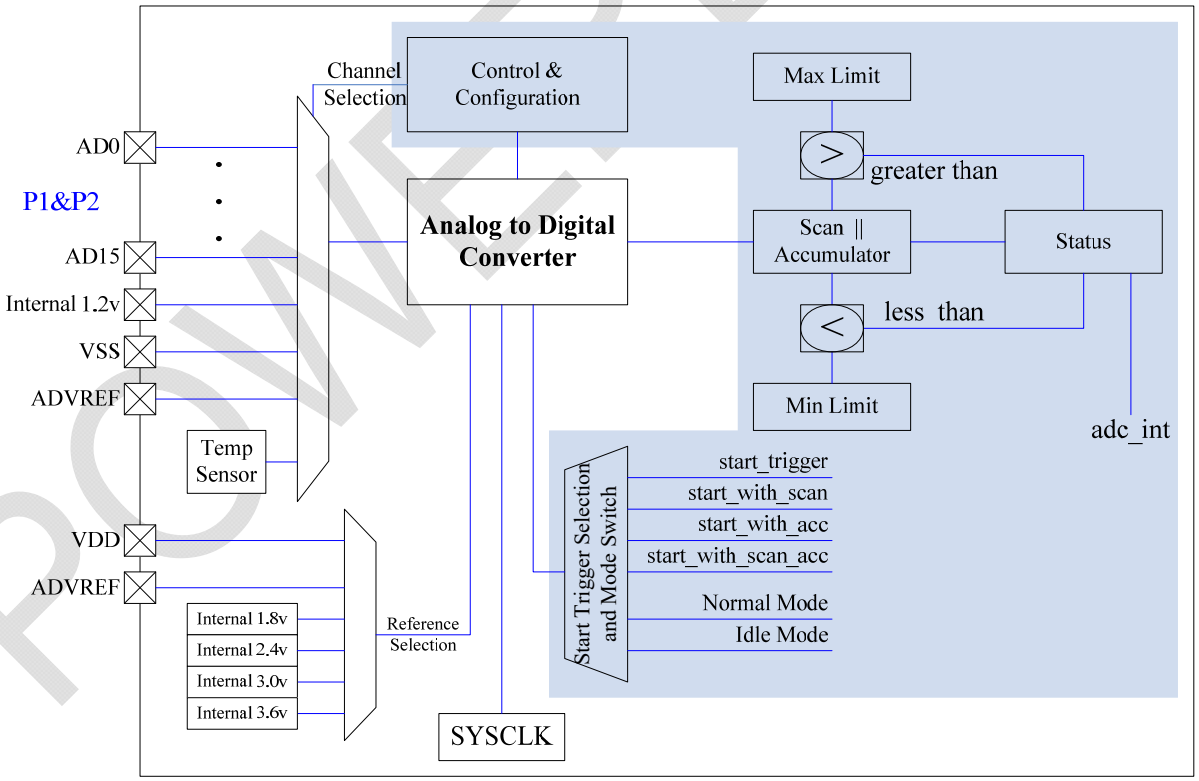


Figure 26-1 ADC&TSC Function Diagram

26.1.1 ADC Operation

The device contains 15 ADC inputs which are shared with logical I/O pins, with the desired function selected using register bits. The ADC module also has its own interrupt vectors and set of interrupts flags.

26.1.2 ADC Interrupt

ADC interrupt could be triggered by ADC data is ready to read, or be triggered by the end of all the session done.

The session done for ADC is defined as the end of accumulation if accumulation is enabled, or the end of channel scan if scan is enabled, or end of both of accumulation and channel scan if they are enabled both.

26.1.3 ADC Work Mode

The modes in which the design supports to configure to work lists at the following table:

Table 26-1 ADC Work Mode

Mode	Key	Polling	Accumulation	Interrupt Source	Work Mode States
Normal /IDLE	single	X	N	Data ready to read or overflow	trig_sel: 0 – Single channel single conversion, generating interrupt after completion of data conversion; 1 – Continue to work，generating interrupt when the single channel is judged to be cross threshold action(compare with the threshold of single channel);
Normal /IDLE	single	X	Y	Data ready to read or overflow	trig_sel: 0 – Multiple conversion with single channel, accumulating the converted data, generating interrupt when the number of times is reached; 1 – Continue to work, generating interrupt when the single channel is judged to be multiple accumulating cross threshold action(compare with the accumulation threshold of single channel);
Normal /IDLE	Comb *	N	N	Data ready to read or overflow	trig_sel: 0 – Single channel (lowest channel) single conversion, generating interrupt after completion of data conversion;

Mode	Key	Polling	Accumulation	Interrupt Source	Work Mode States
					1 – Continue to work，generating interrupt when the single channel (lowest channel) is judged to be cross threshold action(compare with the threshold of single channel);
Normal /IDLE	Comb	N	Y	Data ready to read or overflow	trig_sel: 0 –Multiple conversion with single channel (lowest channel), accumulating the converted data, generating interrupt when the number of times is reached; 1 – Continue to work, generating interrupt when the single channel (lowest channel) is judged to be multiple accumulating cross threshold action (compare with the accumulation threshold of single channel);
Normal /IDLE	Comb	Y	N	Data ready to read or overflow	trig_sel: 0 – Polling each selected channels single conversion, generating interrupt after completion of each data conversion; 1 –Continue to work，generating interrupt when polling each selected channels is judged to be cross threshold action(compare with the shared threshold of combined channels);
Normal /IDLE	Comb	Y	Y	Data ready to read or overflow	trig_sel: 0 –Polling each selected channels multiple conversion, after completion of multiple conversion; generating interrupt when the number of times is reached; 1 –Continue to work，generating interrupt when polling some channel of selected channels is judged to be multiple accumulating cross threshold action(compare with the shared accumulation threshold of combined channels);

Note1: *Combined channels depend the selected channel

Note2: Configure ADCON0.0 (scan_mode) can enter scaning mode

Note3: Configure ADCON1.6 (accum_sel) can select accumulate mode

26.2 Register Definition

26.2.1 ADC Registers Address Map

Table 26-2 ADC Registers Address Map

Name	SFR Address	Bit width	Function states
ADDATL	0xD1	8	ADC data low 8 bits
ADDATH	0xD2	8	ADC data high 8 bits
ADOUTL	0xCE	8	ADC direct output data low 8 bits
ADOUTH	0xCF	3	ADC direct output data high 3 bits
ADCHS0	0xD3	8	ADC channels select register 0
ADCHS1	0xD4	8	ADC channels select register 1
ADCON0	0xD5	8	ADC control register 0
ADCON1	0xD6	8	ADC control register 1
ADCON2	0xD7	8	ADC control register 2
ADSTA	0xDD	8	ADC status register
ADCSOF	0xDF	8	ADC status register
ADWKL0	0xD9	8	ADC wakeup threshold 0 low 8 bits
ADWKH0	0xDA	8	ADC wakeup threshold 0 high 8 bits
ADWKL1	0xDB	8	ADC wakeup threshold 1 low 8 bits
ADWKH1	0xDC	8	ADC wakeup threshold 1 high 8 bits

26.2.2 ADC Data Register – ADDATL

Table 26-3 ADDATL Register (D1h)

Bit	Symbol	Description	Type	Reset
addatl.7~0	-	When 'adc_en' is set, the register store the ADC low 8bits data; When 'tsc_en' is set, the register store the temperature sensor low 8bits data;	R/W	00h

26.2.3 ADC Data Register – ADDATH

Table 26-4 ADDATH Register (D2h)

Bit	Symbol	Description	Type	Reset

Bit	Symbol	Description	Type	Reset
addath.7~0	-	When 'adc_en' is set, the register store the ADC high 8bits data; When 'tsc_en' is set, the register store the temperature sensor high 8bits data;	R/W	00h

26.2.4 ADC Data Direct Output Register – ADOUTL

Table 26-5 ADOUTL Register (CEh)

Bit	Symbol	Description	Type	Reset
adoutl.7~0	-	When 'adc_en' is set, the register store the ADC low 8bits data; When 'tsc_en' is set, the register store the temperature sensor low 8bits data;	R	00h

26.2.5 ADC Data Direct Output Register – ADOUTH

Table 26-6 ADOUTH Register (CFh)

Bit	Symbol	Description	Type	Reset
adouth.7	-	-Reserved, must keep in 0.	TW	1'b0
adouth.6	ADC_EN2RUN	ADC_EN replace ADC_RUN enable When is set, enable	TW	1'b0
adouth.5~3		Reserved	R	3'b0
adouth.2~0	-	When 'ADC_EN' is set, the register store the ADC high 3bits data; When 'TSC_EN' is set, the register store the temperature sensor high 3bits data;	R	3'b0

26.2.6 ADC select Register – ADCHS0

Table 26-7 ADCHS0 Register (D3h)

Bit	Symbol	Description	Type	Reset
adchs0.7~0	-	ADC 7~0 channel select bit (small sample switch resistance)	R/W	00h

26.2.7 ADC select Register – ADCHS1

Table 26-8 ADCHS1 Register (D4h)

Bit	Symbol	Description	Type	Reset
adchs1.7~0	-	ADC15~8 channel select bit (large sample switch resistance)	R/W	00h

26.2.8 ADC control Register – ADCON0

Table 26-9 ADCON0 Register (D5h)

Bit	Symbol	Description	Type	Reset
adcon0.7	-	Reserved, must keep in 0.	R/W	1'b0
adcon0.6	adc_en	If set ADC convert is enabled, otherwise, ADC convert is disabled	R/W	1'b0
adcon0.5	tsc_en	If set TSC mode is enabled, when adc_en=0, TSC mode can be set by setting tsc_en=1.	R/W	1'b0
adcon0.4	wait_rd_en	If set, wait till CPU to read out the data at present, then start the next ADC probe operation.	R/W	1'b0
adcon0.3	freq_sel2	ADC analog clock frequency prescaler of system clock select options: 3'b000: no prescaler 3'b001: prescaler by 2 3'b010: prescaler by 4 3'b011: prescaler by 8 3'b100: prescaler by 16 3'b101: prescaler by 32 3'b110: prescaler by 64 3'b111: prescaler by 128	R/W	3'b0
adcon0.2	freq_sel1			
adcon0.1	freq_sel0			
adcon0.0	scan_mode	When ADC function is enabled, this bit select the ADC work mode, if set scanning mode is selected, otherwise, scanning mode is closed	R/W	1'b0

26.2.9 ADC control Register – ADCON1

Table 26-10 ADCON1 Register (D6h)

Bit	Symbol	Description	Type	Reset

Bit	Symbol	Description	Type	Reset
adcon1.7	start	If set, trigger the ADC function start working, in the end of the operation, this bit will be auto cleared and wait the next start trigger.	R/W	1'b0
adcon1.6	accum2	**Accumulative number:** 3'h0: single time convert data 3'h1: accumulate 2 times convert data 3'h2: accumulate 4 times convert data 3'h3: accumulate 8 times convert data … 3'h7: accumulate 128 times convert data Note: please configure the accumulation time carefully to avoid the overflow of sum, if overflow, the 'ACCUM_OVF' will be set to indicates the bad accumulation.	R/W	3'b0
adcon1.5	accum1			
adcon1.4	accum0			
adcon1.3	ave_dis	**Average operation disable** If set, disable average operation, otherwise, enable average operation	R/W	1'b0
adcon1.2	trig_sel	In the normal/idle work mode, when configure as ADC function, interrupt could be triggered by two sources: 1'b0: ADC data is valid and trigger interrupt 1'b1: ADC cross threshold overflow action trigger interrupt	R/W	1'b0
adcon1.1	-	Reserved Keep in 1, the design is working as ADC function.	R/W	1'b0
adcon1.0	accum_ovf	Indicates the overflow is occurred in the accumulative operation	R/W	1'b0

26.2.10 ADC control Register – ADCON2

Table 26-11 ADCON2 Register (D7h)

Bit	Symbol	Description	Type	Reset
adcon2.7	lslp_mode	Low speed mode low power enable If set, enable low speed ADC conversation mode reduce power consumption	R/W	1'b0
adcon2.6	ses_gap2	The gap time between two session of accumulation operation, configure as: 3'h0: 0 clock period of 'clk_32k' 3'h1: 8 clock period of 'clk_32k' (0.25ms) 3'h2: 32 clock period of 'clk_32k' (1ms) 3'h3: 128 clock period of 'clk_32k' (4ms) 3'h4: 256 clock period of 'clk_32k' (8ms)	R/W	3'b0
adcon2.5	ses_gap1			

adcon2.4	ses_gap0	3'h5: 512 clock period of 'clk_32k' (16ms) 3'h6: 1024 clock period of 'clk_32k' (31ms) 3'h7: 2048 clock period of 'clk_32k' (62ms)		
adcon2.3	idle_run_flag	idle start flag, indicates the process triggered by previous go-idle command is not finished yet, and the next step will be continue after coming go-idle command, this bit will be auto-cleared by hardware when end of process, it also could be cleared by CPU	R/W	1'b0
adcon2.2	wait_rd_flag	Wait CPU flag, indicates process is handling wait for CPU read, it should be cleared by CPU setting 1'b0 after read out data.	R/W	1'b0
adcon2.1	sta_gap1	The gap time between two start trigger, configure as: 2'b00: 2 clock period of 'adc_clk' 2'b01: 4 clock period of 'adc_clk' 2'b10: 8 clock period of 'adc_clk' 2'b11: 16 clock period of 'adc_clk'	R/W	2'b0
adcon2.0	sta_gap0			

26.2.11 ADC status Register – ADSTA

Table 26-5 ADSTA Register (DDh)

Bit	Symbol	Description	Type	Reset
adsta.7	inject	If set, injection operation is enabled, wait the current normal channel conversion is finished and channel 15 is injected into ADC to start conversion until this bit is cleared, then return to the channel which is interrupted. Note: this bit just set or clear by software	R/TW	1'b0
adsta.6	adc_pump	1:support VDD50 higher than 2.4V, lower than 2.7V; 0:support VDD50 higher than 2.7V;	R/W	1'b0
adsta.5	iref_adj1	2'b00:1uA; 2'b01:2uA; 2'b10:4uA; 2'b11:6uA;	R/W	2'b0
adsta.4	iref_adj0			
adsta.3	adc_ccm	**ADC continuous conversion mode** 0: disable continuous conversion mode 1: enable continuous conversion mode	R/W	1'b0
adsta.2	adc_vref2	**ADC reference select:** 3'b00x:VDD pin;	R/W	3'b0

Bit	Symbol	Description	Type	Reset
adsta.1	adc_vref1	3'b01x: ADVREF pin; 3'b100: internal 1.8V; 3'b101: internal 2.4V; 3'b110: internal 3.0V; 3'b111: internal 3.6V;		
adsta.0	adc_vref0			

Note:

Bit adsta.3(adc_ccm) is used for ADC continuously convert mode only, and for other usage is forbidden. And it must be set before the 'adcon1.7'(start) is set. the following steps should be obeyed for ADC continuously convert mode:

Step1: ORL ADSTA, #008H // trigger ADC continuously mode start 'acc_ccm'

Step2: ORL ADCON0, #040H // enable ADC mode

Step3: ORL ADCON1, #080H // trigger ADC start

Step4: // wait until ADC interrupt comes and get the ADC convert data from 'addath', 'addatl'

Step5: // cleared ADC continuously mode start 'acc_ccm' if it the ADC data is enough and then clear 'adc_en'

26.2.12 ADC status Register – ADCSOF

Table 26-13 ADCSOF Register (DFh)

Bit	Symbol	Description	Type	Reset
adcsof.7	-	Reserved	R/W	1'b0
adcsof.6	cpol	Select the polarity of comparison between convert data and wakeup threshold value configured into 'adwk0/adwk1': 1'b0: involves interrupt when data is more than 'adwk1' or less than 'adwk0' (X≤adwk0 or X≥adwk1) 1'b1: involves interrupt when data is less than 'adwk1' and more than 'adwk0' (adwk0≤X≤adwk1)	R/W	1'b0
adcsof.5	ch_sw1	Four type sources could be select as ADC channel: 2'b00: switch to P1&P2, configure 'adchs1[7:0]' to select any P2.7~P2.0 as channel, configure 'adchs0[7:0]' to select any P1.7~P1.0 as channel; 2'b01: switch to internal 1.2v; 2'b10: switch to ground (0v); 2'b11: switch to reference source Note: when adc_en=1, need to configure TKCHS0 or TKCHS1 as not all 0 value, ADC interrupt can response normally.	R/W	2'b0
adcsof.4	ch_sw0			

Bit	Symbol	Description	Type	Reset
adcsof.3~0	escap_ofst3~0	**ADC Extra Sampling Capacitance Selection** 0000 = Inhibit extra sampling capacitance 0001 = Extra sampling capacitance is 2 pF 0010 = Extra sampling capacitance is 4 pF 0011 = Extra sampling capacitance is 6 pF 0100 = Extra sampling capacitance is 8 pF 0101 = Extra sampling capacitance is 10 pF 0110 = Extra sampling capacitance is 12 pF 0111 = Extra sampling capacitance is 14 pF 1000 = Extra sampling capacitance is 16 pF 1001 = Extra sampling capacitance is 18 pF 1010 = Extra sampling capacitance is 20 pF 1011 = Extra sampling capacitance is 22 pF 1100 = Extra sampling capacitance is 24 pF 1101 = Extra sampling capacitance is 26 pF 1110 = Extra sampling capacitance is 28 pF 1111 = Extra sampling capacitance is 30 pF	R/W	4'hF

26.2.13 ADC Wakeup threshold Register – ADWKL0

Table 26-6 ADWKL0 Register (D9h)

Bit	Symbol	Description	Type	Reset
adwkl0.7~0	-	When 'adc_en' is set, the register store the ADC limit 0 threshold low 8bits data; When 'tsc_en' is set, the register store the TSC limit 0 threshold low 8bits data;	R/W	00h

26.2.14 ADC Wakeup threshold Register – ADWKH0

Table 26-7 ADWKH0 Register (DAh)

Bit	Symbol	Description	Type	Reset
adwkh0.7~0	-	When 'adc_en' is set, the register store the ADC limit 0 threshold high 8bits data; When 'tsc_en' is set, the register store the TSC limit 0 threshold high 8bits data;	R/W	00h

26.2.15 ADC Wakeup threshold Register – ADWKL1

Table 26-8 ADWKL1 Register (DBh)

Bit	Symbol	Description	Type	Reset
adwkl1.7~0	-	When 'adc_en' is set, the register store the ADC limit 1 threshold low 8bits data; When 'tsc_en' is set, the register store the TSC limit 1 threshold low 8bits data;	R/W	00h

26.2.16 ADC Wakeup threshold Register – ADWKH1

Table 26-17 ADWKH1 Register (DCh)

Bit	Symbol	Description	Type	Reset
adwkh1.7~0	-	When 'adc_en' is set, the register store the ADC limit 1 threshold high 8bits data; When 'tsc_en' is set, the register store the TSC limit 1 threshold high 8bits data;	R/W	00h

27 AUX Control Register

27.1 Overview

AUXCON control register, reserved bit must keep in 0.

27.2 Register Defination

27.2.1 AUX Control Register–AUXCON

Table 27-1 AUXCON Register (E8h)

Bit	Symbol	Description	Type	Reset
auxcon.7	extcap_en	**TKVREF external capacitor enable** 0：disable 1：enable	R/TW	0
auxcon.6	-	**Reserved, must keep in 0**	R/TW	0
auxcon.5	-	**Reserved, must keep in 0**	R/W	0
auxcon.4	-	**Reserved, must keep in 0**	R/W	0
auxcon.3	s003_sopt	**S003(UART/SPI/I2C) compatible pin enable** 0 – incompatible 1 – compatible	R/TW	0
auxcon.2	-	**Reserved**	R	0
auxcon.1	-	**Reserved**	R	0
auxcon.0	-	**Reserved, must keep in 0**	R/W	0

28 Analog Comparator

28.1 Overview

The device is provided one analog comparator. Input and output options allow use of the comparator in a number of different configurations. The comparator output is a logical one when its positive input is greater than its negative input, otherwise the output is a zero. The comparator can be configured to cause to an interrupt when the output value change. The block diagram is as below.

The comparator has two control registers CMPCON0 and CMPCON1, Both Inputs are CMP1, CMP2, CMPVREF and internal reference voltage, and output is CMPOUT. After enable comparator the comparator need waited stable time to guarantee comparator output.

The value of internal reference voltage (Vref) is 1.2V (+/-2%, @25°C).

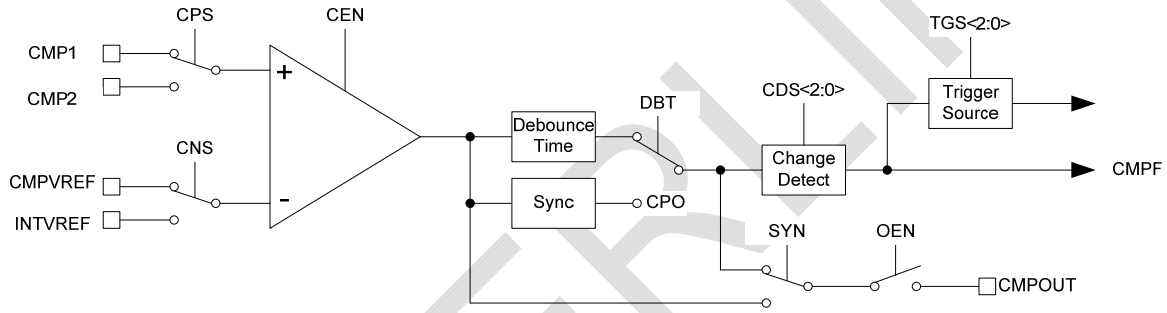


Figure 28-1 Analog Comparator

28.2 Register Definition

28.2.1 Comparator Control Register 0 – CMPCON0

Table 28-1 CMPCON0 Register (BFh)

Bit	Symbol	Description	Type	Reset
cmpcon0.7	cen	**Comparator enable** 0: Disable Comparator 1: Enabled Comparator	R/W	0
cmpcon0.6	cps	**Comparator positive input select** 0: CMP1 is selected as the positive comparator input 1: CMP2 is selected as the positive comparator input	R/W	0
cmpcon0.5	cns	**Comparator negative input select** 0: CMPVREF is selected as the negative comparator input	R/W	0

Bit	Symbol	Description	Type	Reset
		1: INTVREF is selected as the negative comparator input		
cmpcon0.4	oen	**Comparator output enable** 1: CMPOUT output is enabled if CEN = 1 0: CMPOUT output is disabled	R/W	0
cmpcon0.3	cpo	**Comparator output** Synchronized to CPU clock to allow reading by software. Cleared when the comparator is disabled (CEN = 0).	R/W	0
cmpcon0.2	dbt	**Comparator debounce time enable** 1: enable 8 system clocks debounce time 0: disable debounce time, only synchronous	R/W	0
cmpcon0.1	syn	**Comparator synchronous/asynchronous selection** 1: synchronous output 0: asynchronous output	R/W	0
cmpcon0.0	hsy	**Comparator voltage hysteresis function enable** 0: disable 1: enable	R/W	0

28.2.2 Comparator Control Register 1 – CMPCON1

Table 28-2 CMPCON1 Register (BEh)

Bit	Symbol	Description	Type	Reset
cmpcon1.7	tgs3	**Comparator trigger source selection**	R/W	0
cmpcon1.6	tgs2		R/W	0
cmpcon1.5	tgs1		R/W	0
cmpcon1.4	tgs0		R/W	0
cmpcon1.3	vref_en	Internal vref12 enable, if set, vref12 enabled, if you intend to select internal vref12 as one reference voltage to compare, this bit should be set before the 'cen' is set for the reason that internal vref12 stable time is about 60us.	R/W	0
cmpcon1.2	cds2	**Comparator interrupt change detect selection**	R/W	0
cmpcon1.1	cds1		R/W	0
cmpcon1.0	cds0		R/W	0

Table 28-3 Comparator Interrupt Change Selection

CDS2	CDS1	CDS0	Comparator Interrupt Change Detect Selection
0	0	0	Low level
0	0	1	High level

CDS2	CDS1	CDS0	Comparator Interrupt Change Detect Selection
0	1	0	Falling Edge
0	1	1	Rising Edge
1	0	0	Toggle
1	0	1	-
1	1	0	-
1	1	1	-

Table 28-4 Comparator Trigger Source Selection

TGS3	TGS2	TGS1	TGS0	Comparator Trigger Source Selection
0	1	0	0	Trigger Timer 2 Capture Operation
0	1	0	1	Switch-on PWM0 output, set PWM0EN
0	1	1	0	Switch-on PWM1 output, set PWM1EN
0	1	1	1	Switch-on all PWMx output, set all PWMxEN
1	0	0	0	Switch-off PWM2 output, clear PWM2EN
1	0	0	1	Switch-off PWM3 output, clear PWM3EN
1	0	1	0	Switch-off PWM4 output, clear PWM4EN
1	0	1	1	Switch-off PWM5 output, clear PWM5EN
1	1	0	0	Switch-on PWM2 output, set PWM2EN
1	1	0	1	Switch-on PWM3 output, set PWM3EN
1	1	1	0	Switch-on PWM4 output, set PWM4EN
1	1	1	1	Switch-on PWM5 output, set PWM5EN

29 Flash & EEPROM

The memory contains 16K bytes program Flash code area, 256 bytes data EEPROM code area.

- 16K bytes program Flash
- 256 bytes data EEPROM (page/byte operation)

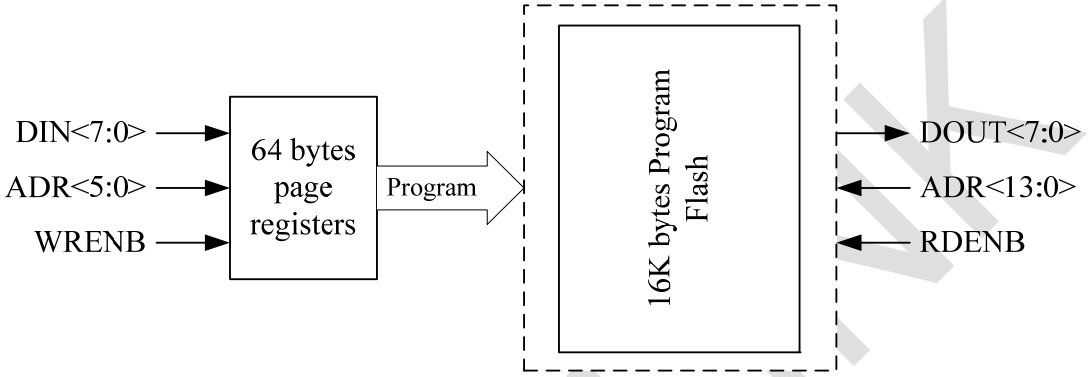


Figure 29-1 Flash Area

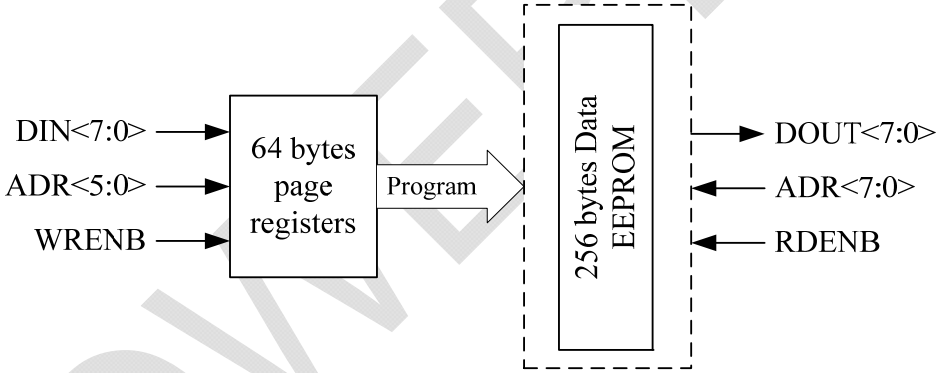


Figure 29-2 EEPROM Area

29.1 Memory Encryption

The program code area of Flash is encrypted in this device.

29.2 Register Definition

29.2.1 EEPROM Control Register – EECON

Table 29-1 EECON Register (97h)

Bit	Symbol	Description	Type	Reset
eecon.7	LOCK	**EEPROM program inhibit** 0 – EEPROM program is enabled 1 – EEPROM program is inhibited	R/W	0
eecon.6	-	**-**	R	0
eecon.5	-	**-**	R	0
eecon.4	-	**-**	R	0
eecon.3	EPGM	**EEPROM program interrupt enable** When epgm=0 EEPROM program interrupt is disabled. When epgm=1 and ea=1 EEPROM program interrupt is enabled.	R/W	0
eecon.2	PGMF	**EEPROM program interrupt flag** 1 – EEPROM program is finished It can only be set by hardware and can be cleared by software or interrupt. When set PGM to 1, it will be cleared automatically.	R/W	0
eecon.1	CPF	**EEPROM program cross page flag** 1 – EEPROM program page is changed (cross page) If CPF=1, PGM can not be set to 1 until CPF is cleared by software. CPF can only be set to 1 by hardware; it can not be set to 1 by software. After cross page error occurred, more than 3 NOP must be followed close behind the CPF cleared instruction to avoid the reset operation of EEPROM.	R/W	0
eecon.0	PGM	**EEPROM program enable** 1 – start EEPROM program After write data to EEPROM buffer, set it to start EEPROM program. If EEPROM buffer is not written, software can not set it. When program is finished, it is cleared by hardware automatically. It can not be cleared by software.	R/TW	0

30 ICP (In-Circuit Programming)

30.1 Overview

The contexts of flash in the device are empty by default. User must program the flash by external Writer device or by ICP (In-Circuit Programming) tool.

In the ICP tool, the user must take note of ICP's programming pins used in system board. In some application circuits, it is highly recommended customer power off then power on after ICP programming has completed on the system board.

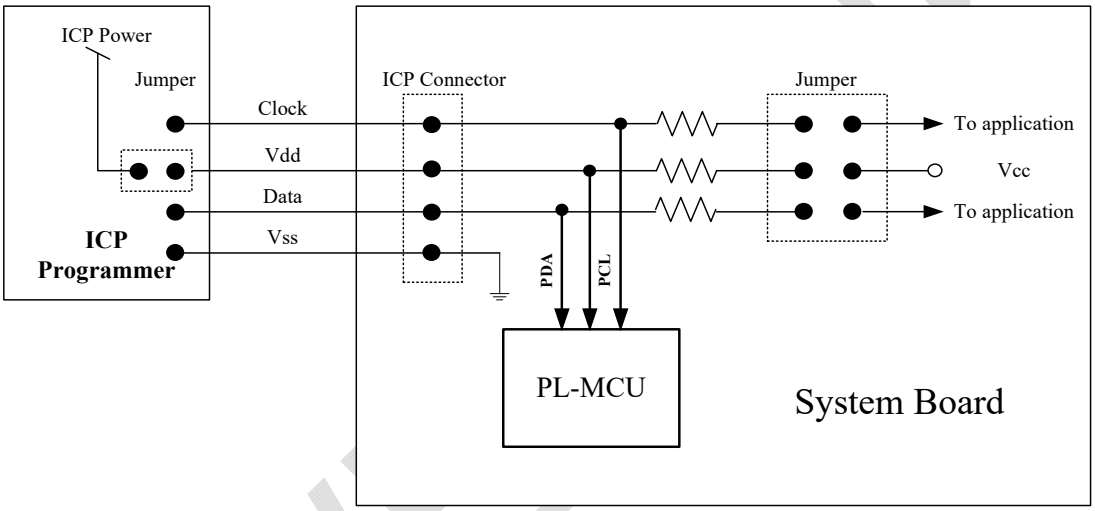


Figure 30-1 ICP Application Circuit

Note:

1. Circuitry separation is optionally needed between ICP and application during ICP operation.
2. Resistor is optional by application
3. When using ICP to upgrade code, the clock PCL and data PDA must be taken within design system board.
4. After program finished by ICP, to suggest system power must power off and remove ICP connector then power on.

The device supports programming of Flash (16K bytes AP Flash), and data EEPROM (256 bytes). User has the option to program the AP Flash and data EEPROM either individually or both.

31 ICD (In-Circuit Debugging)

31.1 Overview

The ICD implements functions which allow to stop/run/step the CPU.

- 2-pin access to your on-chip
- Efficient use of the 2-pin interface for both test and debug

ICD debug pin PCL and PDA can be controlled by enabling Option bit CODE1.7(ICDEN); When CODE1.7 is 0, the ICD debug pin disabled; When CODE1.7 is 1, enable ICD debug pin, PCL and PDA are dedicated to ICD debug.

32 Config Options

The config options are used for code configuration.

Config Option	Config Option
Program area Flash lock 0 – Lock 1 – Unlock	**Data area EEPROM lock** 0 – Lock 1 – Unlock
Flash ROM area enable 0 – Does not cure into ROM 1 – Cured into ROM	**Flash ROM area size select** 0 – High 4K as ROM area 1 – High 8K as ROM area
RSTB reset pin enable 0 – Disable 1 – Enable	**ICD debug pin enable** 0 – Disable 1 – Enable
Oscillator type select 00 – Internal high frequency RC (4~12MHz) 01 – Internal low frequency RC (32KHz) 10 – Crystal and ceramic oscillator XTAL 11 – External clock input ECLK	**Internal high frequency RC frequency select** 00 – Internal RC 4MHz 01 – Internal RC 8MHz 10 – Internal RC 12MHz 11 – RSV
XTAL crystal internal res/cap config 0 – Nonuse 15pf internal cap. and feedback res. 1 – Use 15pf internal cap. And feedback res.	**XTAL crystal drive gear adaptation** 000 – 200KHz 001 – 400KHz 010 – 2MHz 011 – 4MHz 100 – 8MHz 101 – 12MHz 110 – RSV 111 – RSV
External clock ECLK config code 00 – LECK low power mode(0MHz~0.5MHz) 01 – MECK medium power mode(0.5MHz~4MHz) 10 – HECK high power mode(4MHz~12MHz) 11 – HECK high power mode(4MHz~12MHz)	
Warm-start time config 00 – The longest …… 11 – The shortest *Note: different oscillators Warmup gears different*	**Timeout config** 00 – (16ms+4*4ms retry)*2----------64ms 01 – (16ms+4*4ms retry)+16ms-------48ms 10 – (16ms+4*4ms retry)+8ms---------40ms 11 – (16ms+4*4ms retry)+0.125ms----32ms
WDT enable 0x – Disable 10 – Enable, control by WDTEN 11 – Enable, control by WDTEN, disable in stop mode	**WDT enable power-on default config** 0 – Default disable WDT 1 – Default enable WDT(WDT is enabled)
Low voltage reset LVR enable 00 – disable 01 – RSV 10 – enable(in SLEEP mode need turn on) 11 – RSV	**Low power detect LPD enable** 0 – disable 1 – enable
Low voltage reset LVR threshold voltage select	**Low power detect LPD threshold voltage select**

Config Option	Config Option
000 – 1.2v 001 – 1.5v 010 – 1.8v 011 – 2.1v 100 – 2.4v 101 – 2.7v 110 – 3.7v 111 – 4.3v	000 – 1.2v 001 – 1.5v 010 – 1.8v 011 – 2.1v 100 – 2.4v 101 – 2.7v 110 – 3.7v 111 – 4.3v
External interrupt trigger supplementary mode release mode select 0 – Released by IFx 1 – Released by intxack	
External interrupt 0 triggers the supplement mode select 00 – Default mode, controlled by it0 & it0_inv 01 – Posedge trigger(internal low level trigger) 10 – Negedge trigger(internal low level trigger) 11 – Dual edge trigger(internal low level trigger)	**External interrupt 1 triggers the supplement mode select** 00 – Default mode, controlled by it1 & it1_inv 01 – Posedge trigger(internal low level trigger) 10 – Negedge trigger(internal low level trigger) 11 – Dual edge trigger(internal low level trigger)

33 Electrical Characteristics

33.1 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage and affect device reliability if exceeded.

Parameter	Symbol	Min.	Max.	Unit
DC Power Supply	VDD-VSS	-0.3	+6.0	V
Input Voltage	V_{IN}	VSS-0.3	VDD+0.3	V
Operating Temperature	T_A	-25	+125	°C
Storage Temperature	T_{ST}	-55	+150	°C
Maximum Current into VDD			120	mA
Maximum Current out of VSS			120	mA
Maximum Current suck by a I/O pin			25	mA
Maximum Current sourced by a I/O pin			25	mA
Maximum Current suck by total I/O pins			75	mA
Maximum Current sourced by total I/O pins			75	mA

Note: These are stress ratings only. Stress beyond these limits may cause permanent damage to the device. Functional operation of the device at these or any conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.

33.2 DC Electrical Characteristics

(VDD = 2.4V~5.5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Specification				Test Conditions
		Min.	Typ.	Max.	Units	
Operating Voltage	VDD	2.4		5.5	V	
Operation Current	I_{OP}		5		mA	No load, VDD=5V@12MHz
IDLE Current	I_{IDLE}		2.5		mA	No load, VDD=5V@12MHz, IDLE
Power Down Current	I_{STOP}		5		uA	No load, VDD=5V@12MHz, STOP
Power Down Current	I_{SLEEP}		3		uA	No load, VDD=5V@12MHz, Sleep
Input High Voltage	V_{IH}	0.7*VDD		VDD+0.2	V	
Input Low Voltage	V_{IL}	-0.5		0.3*VDD	V	
Output High Voltage	V_{OH}	2.5	3.5		V	VDD=4.5V, I_{OH}=-20mA
Output Low Voltage	V_{OL}		0.5	0.7	V	VDD=4.5V, I_{OL}=+20mA
Port Pull up Resistor	R_{PU}		100		KΩ	
POR slope rate	S_{POR}	0.025		4.5	V/ms	
POR threshold voltage of rising	V_{PORH}		1.6		V	
POR threshold voltage of falling	V_{PORL}		1.2		V	
POE threshold voltage	V_{POE}		1.4		V	
Comparator Reference Voltage	Vref	1.176	1.20	1.224	V	T_A = 25°C

33.3 AC Electrical Characteristics

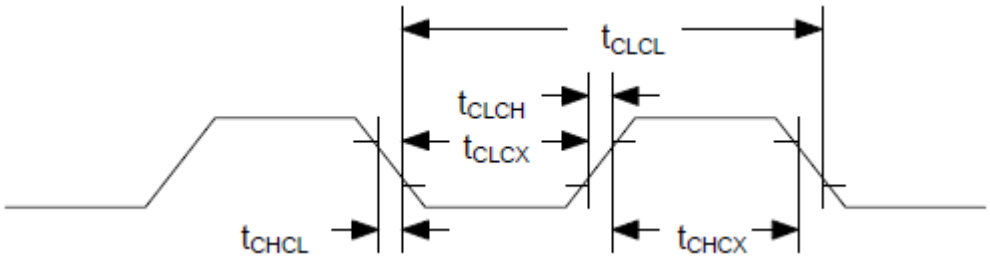


Figure 33-1 Clock Timing

Note: Duty cycle is 50%.

33.3.1 External Clock Characteristics

(VDD = 2.4V~5.5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Specification				Test Conditions
		Min.	Typ.	Max.	Units	
Clock Frequency			12		MHz	
Clock High Time	t_{CHCX}	30			ns	
Clock Low Time	t_{CLCX}	30			ns	
Clock Rise Time	t_{CLCH}			10	ns	
Clock Fall Time	t_{CHCL}			10	ns	

33.3.2 Internal RC OSC Characteristics

(VDD = 2.4V~5.5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Specification				Test Conditions
		Min.	Typ.	Max.	Units	
Clock Frequency			8/12		MHz	
Clock Frequency			±2		%	T_A = 25°C@8MHz

33.3.3 Crystal Oscillator/Ceramic Resonator Characteristics

(VDD = 2.4V~5.5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Specification				Test Conditions
		Min.	Typ.	Max.	Units	
Clock Frequency		400K		12M	Hz	

33.4 Comparator Electrical Characteristics

TA = 25°C, VCC = 2.4V to 5.5V (unless otherwise noted)

Parameter	Symbol	Specification				Test Conditions
		Min.	Typ.	Max.	Units	
Common mode range comparator inputs	V_{CR}	0		VDD	V	
Comparator response time	T_{RS}		30		ns	
Comparator enable to output valid time	T_{EN}		50		us	

34 Typical Application

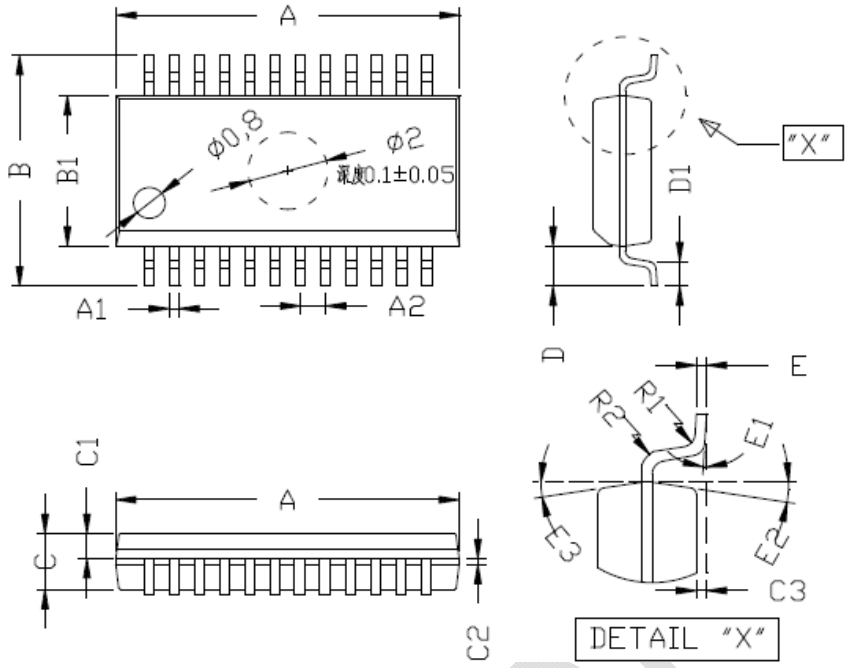
34.1 Intelligent Lighting Demo

N/A

35 Package Dimensions

35.1 SSOP24 Package

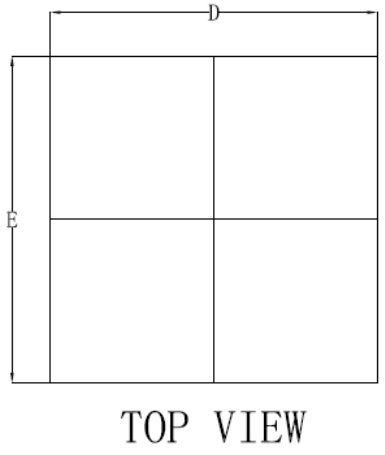
SSOP24 PACKAGE OUTLINE DIMENSIONS



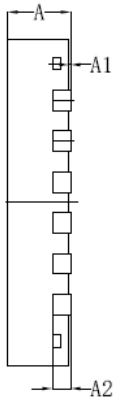
标注	表示	MIN	NOM	MAN
A	总长	8.53	8.63	8.73
A1	脚宽	0.21	0.25	0.30
A2	脚间距		0.635 BSC	
B	跨度	5.80	6.00	6.20
B1	胶体宽度	3.80	3.90	4.00
C	胶体厚度	1.25	1.45	1.55
C1	上胶体厚	0.55	0.65	0.75
C2		0.19	0.20	0.21
C3	站高	0.10	0.15	0.20
D	单边长		1.04 REF	
D1	脚长	0.45	0.60	0.80
E	脚厚		0.25 BSC	
E1	脚角度	0°	4°	8°
E2		6°	8°	10°
E3		6°	8°	10°
R1			0.07 TYP	
R2			0.07 TYP	
h		0.30	0.40	0.50

35.2 QFN24 Package

QFN24 (4*4, P0.50T0.75) PACKAGE OUTLINE DIMENSIONS



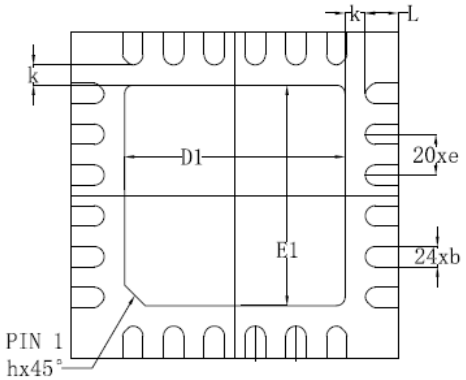
TOP VIEW



SIDE VIEW

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

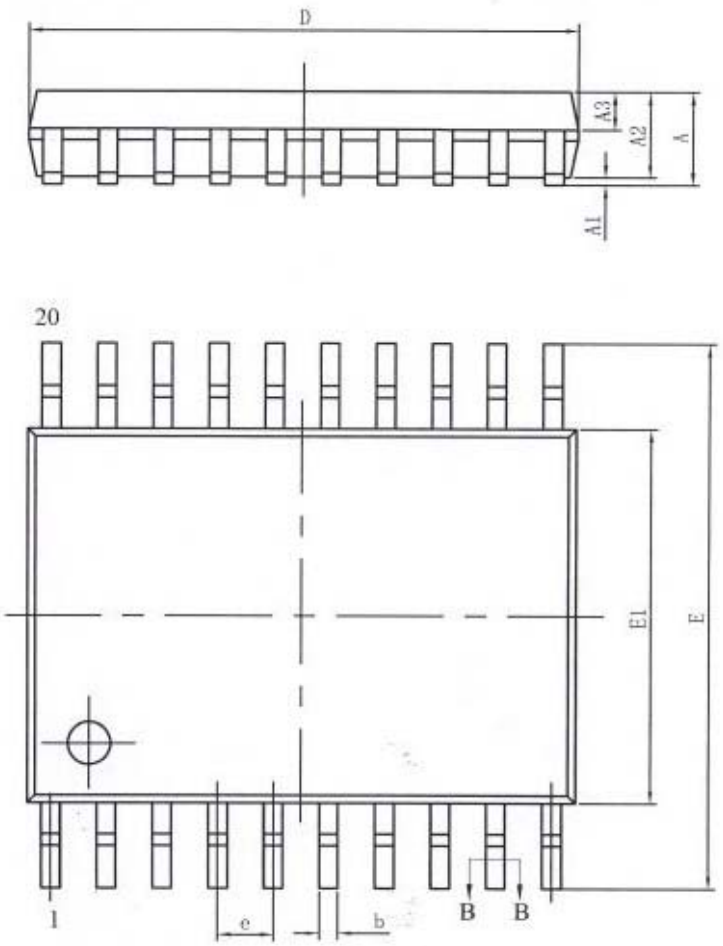
SYMBOL	MIN	NOM	MAX
A	0.700	0.750	0.820
A1	0.000	/	0.050
A2	0.153	0.203	0.273
b	0.200	0.250	0.300
D	3.900	4.000	4.100
D1	2.600	2.700	2.800
E	3.900	4.000	4.100
E1	2.600	2.700	2.800
e	0.450	0.500	0.550
h	0.200	0.250	0.300
k	0.150	0.250	0.350
L	0.350	0.400	0.450



BOTTOM VIEW

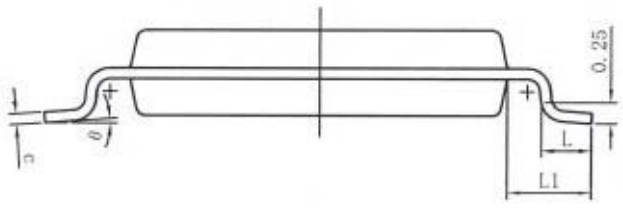
35.3 TSSOP20 Package

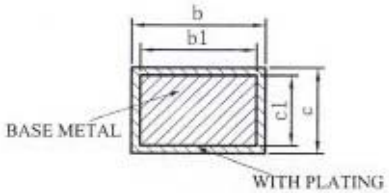
TSSOP20 PACKAGE OUTLINE DIMENSIONS



TSSOP20L

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.29
b1	0.19	0.22	0.25
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	8°

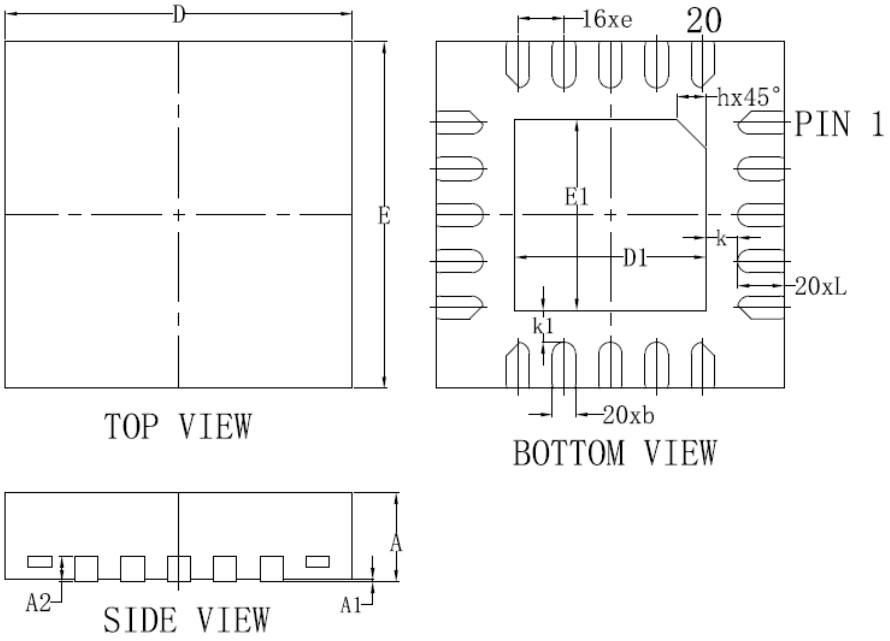




SECTION B-B

35.4 QFN20 Package

QFN20 (3*3, P0.4T0.75) PACKAGE OUTLINE DIMENSIONS

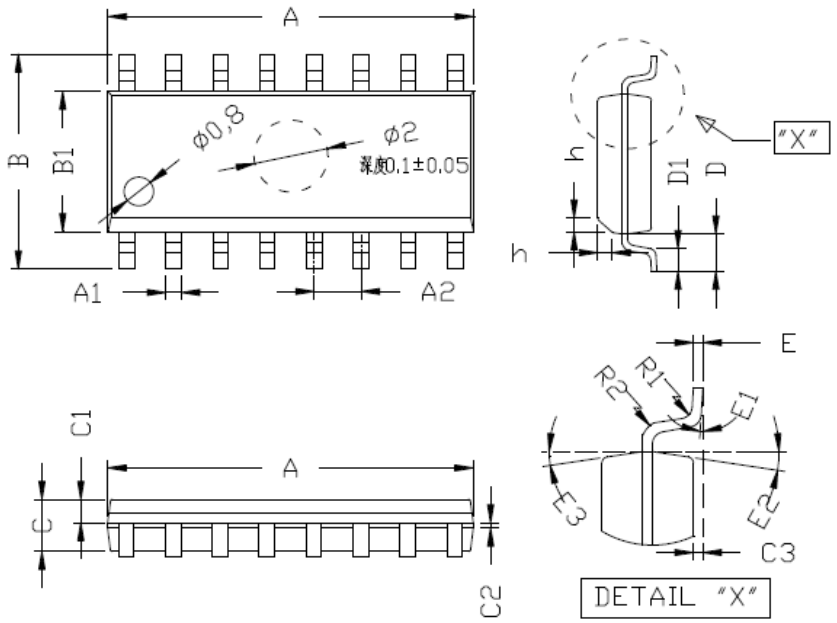


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.700	0.750	0.800
A1	0.000	/	0.050
A2	0.193	0.203	0.233
b	0.150	0.200	0.250
D	2.950	3.000	3.050
D1	1.600	1.650	1.700
E	2.950	3.000	3.050
E1	1.600	1.650	1.700
e	0.350	0.400	0.450
h	0.200	0.250	0.300
k	0.225	0.275	0.325
k1	0.225	0.275	0.325
L	0.350	0.400	0.450

35.5 SOP16 Package

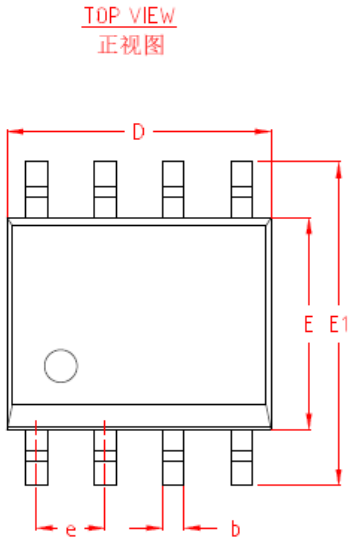
SOP16 PACKAGE OUTLINE DIMENSIONS

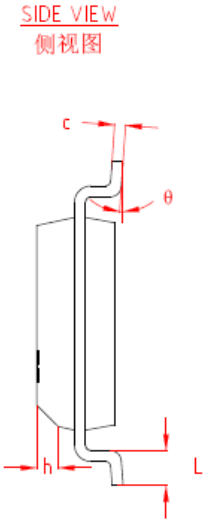


标注	表示	MIN	NOM	MAN
A	总长	9.80	9.90	10.00
A1	脚宽	0.36	0.43	0.51
A2	脚间距		1.27 BSC	
B	跨度	5.80	6.00	6.20
B1	胶体宽度	3.80	3.90	4.00
C	胶体厚度	1.25	1.45	1.55
C1	上胶体厚	0.55	0.65	0.75
C2		0.19	0.20	0.21
C3	站高	0.10	0.15	0.20
D	单边长		1.04 REF	
D1	脚长	0.45	0.60	0.80
E	脚厚		0.25 BSC	
E1	脚角度	0°	4°	8°
E2		6°	8°	10°
E3		6°	8°	10°
R1			0.07 TYP	
R2			0.07 TYP	
h		0.30	0.40	0.50

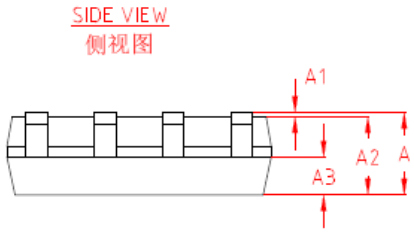
35.6 SOP8 Package

SOP8 PACKAGE OUTLINE DIMENSIONS



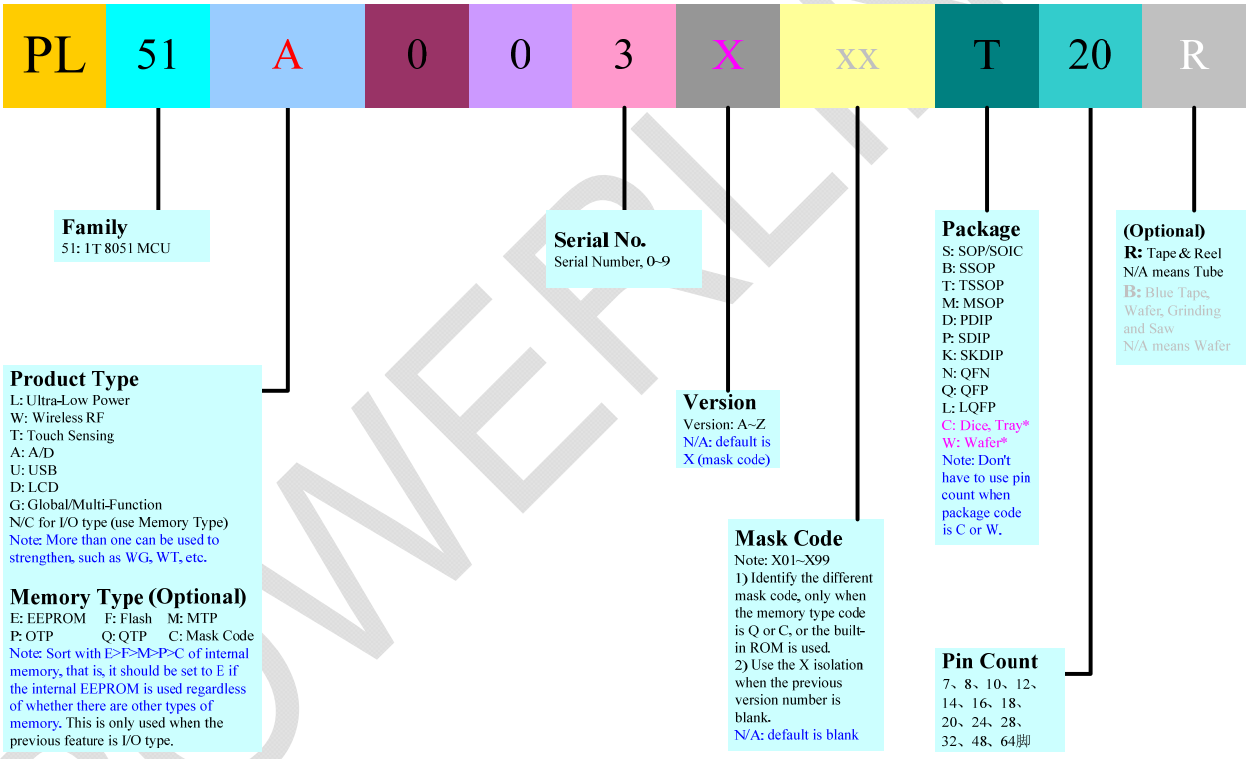


机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	1.50	1.60	1.70
A1	0.04	–	0.12
A2	1.35	1.45	1.55
A3	0.65	0.70	0.75
b	0.35	–	0.50
c	0.19	–	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
e	1.27 BSC		
h	0.30	–	0.50
L	0.50	–	0.80
θ	0°	–	8°



36 Ordering Information

Part Number	Packaging
PL51A003T20	TSSOP20, Tube
PL51A003N20	QFN20, Tube
PL51A003B24	SSOP24, Tube
PL51A003N24	QFN24, Tube
……	……



37 Document Revision History

Rev.	Date	Comments
0.1	2021/02/25	Initial Version
0.2	2021/03/18	Supplement the Description of Product Model Code
0.3	2021/03/26	Updated Ordering Information
0.4	2021/07/30	Revised PWM Common Register Feature
0.5	2021/09/29	Added Register AUXCON.s003_sopt Use Caution
0.6	2021/11/04	Updated Operation Parameter
0.7	2021/11/17	Added package
0.8	2022/07/29	Modified DACCON to AUXCON

38 Important Notice

POWERLINK reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.